Far East Journal of Electronics and Communications
SASTRA Nat. Conf. Elec. Sci. Tech., 2015

http://dx.doi.org/10.17654/EC03010163
Special Issue (March, 2016), Pages 163-170 **ISSN: 0973-7006**

LOW POWER DUAL STACK IN MTCMOS CIRCUITS USING DYNAMIC LOGIC AND SLEEP TRANSISTOR TECHNIQUES

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Abstract

The demand of delivering faster, smaller, and highly reliable integrated circuit chips is what drives the semiconductor market. The most crucial design parameter that requires ultimate attention is power consumption. In the chip design, it is very important to consider the

Received: October 29, 2015; Revised: November 23, 2015; Accepted: December 31, 2015
Keywords and phrases: dual stack, sleep transistor, dynamic logic, DSCH2, micro wind.
Communicated by A. Srinivasan, Guest Editor

factors of power dissipation, operating speed and area. In this paper, the dual stack flip flop circuit is designed in sleep transistor method, dynamic CMOS logic method and pass transistor logic (PTL). The dual stack technique is compared in terms of power area, frequency, dissipation, final voltage and maximum I_{dd} current with sleep transistor method, dynamic logic and PTL logic. The proposed dual stack sleep transistor technique that has reduced leakage power, decreased area among the three logics. The circuit is simulated by DSCH2 CAD tool and layouts are generated by micro wind CAD tools. The circuits are simulated in CMOS 0.12μm technology at 1.2V.

I. Introduction

The main objective of the circuit is to reduce the power consumption and to increase the speed in the dual stack flip flop circuits. The dual stack flip flop circuit is designed with different techniques like sleep transistor method, dynamic CMOS logic method and pass transistor logic (PTL). Their performance is analyzed in terms of power, area, power dissipation, operating speed and leakage current. It is difficult to reduce leakage current during run time, due to the exchange of NMOS transistor and PMOS transistor in the dual stack circuit. The aim is to reduce the power consumption and to increase the speed. It is difficult to reduce leakage current during switching between NMOS transistor and PMOS transistor.

II. Related Works

In the power gating [1] method, a sleep transistor is connected at the actual ground with input signals. This technique provides a considerable reduction in leakage with a least possible impact on chip performance. Here, the high threshold voltage (Vt) PMOS sleep transistors and low threshold voltage (Vt) NMOS sleep transistors compensating the leakage current and thereby reduces the power dissipation. The multi-threshold [2] CMOS technique drastically reduces the leakage of current by removing the idle low threshold voltage of the logic gate devices from the power supply and single phase modulation is another circuitry to the existing sleep transistor which

increases the power consumption and also the area. In this paper, we propose a new technique called dual stack pass transistor technique applied to a SCCER flip-flop network. In the leakage reduction method [3], there is prevention of general sneak leakage path. In the 1V high speed MTCMOS circuit [4], it makes the speed thrice compared to the conventional MTCMOS circuits. In the MTCMOS sequential circuits [5], this method exhibits low leakage current during the standby mode. The twin stack approach [6] shows the minimum value speed power product among all methods. The general multi-threshold circuit is shown in Figure 1:

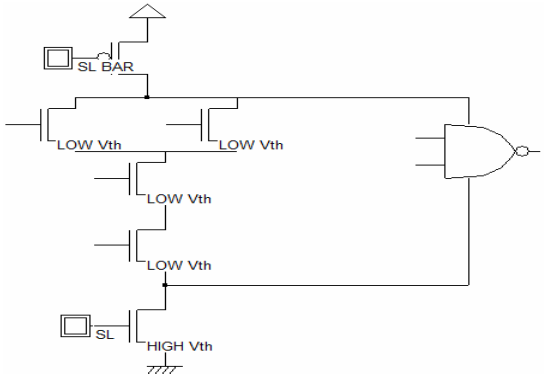

Figure 1. Multi-threshold CMOS circuit.

III. Design Methods - Dual Stack in Sleep Transistor, Dynamic and PTL Method

In dual stack sleep transistor method, the NMOS drain terminal is connected at the leg of the dual stack circuit. The NMOS gate is applied with low input signal and the source terminal is grounded. The NMOS is used to reduce the leakage current and also avoids the power dissipation. Dual stack in dynamic CMOS logic circuit, PMOS and NMOS are connected at the output terminal. Both inputs of the transistors are connected with a common control input, PMOS drain is applied to power supply and NMOS source is connected with ground. In the CMOS logic families, dynamic logic is the fastest logic, so the dual stack dynamic circuit provides high speed. Also, dual stack flip flop circuit is designed in the pass transistor logic (PTL). The

pass transistor logic dual stack circuit shows the less power consumption and the current leakage. Figure 2 is sleep transistor logic. Figure 3 shows dual stack with sleep transistor logic. Figure 4 shows dual stack with dynamic logic and Figure 5 the dual stack with PTL logic.

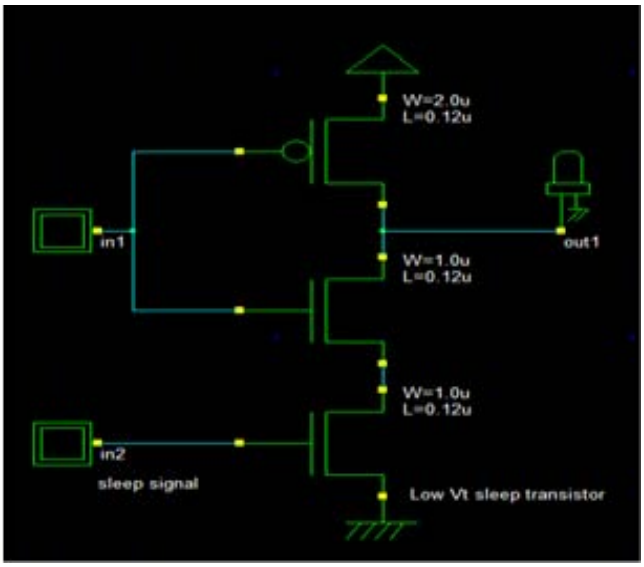

Figure 2. Sleep transistor method.

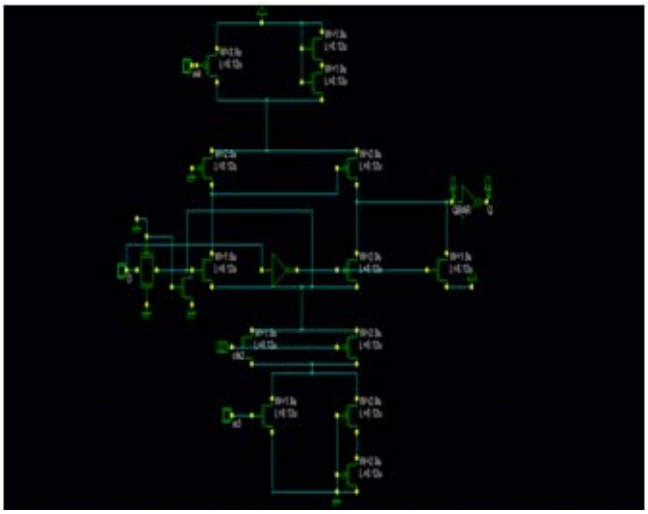

Figure 3. Dual stack with sleep transistor.

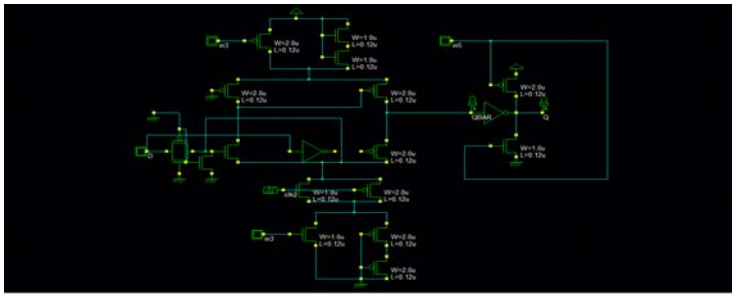

Figure 4. Dual stack in dynamic logic.

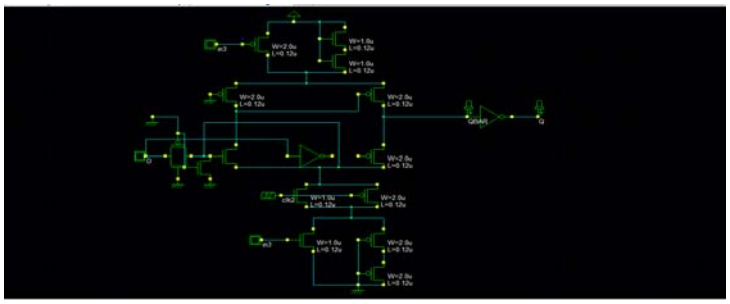

Figure 5. Dual stack in PTL logic.

IV. Table of Results

The table shows the comparison of different parameters such as area, frequency, and power of the two circuits. From the comparison, it is clearly observed that for sleep technique power consumption decreases drastically when comparing to dynamic logic at the same frequency. But the area may be slightly more than dynamic logic. In PTL logic, the power consumption is even more less at a lesser frequency. The maximum I_{dd} current is the least in case of PTL logic.

Parameter	Sleep technique	PTL logic	Dynamic logic
Area	38×14μm	36×14μm	40×9μm
Power	2.849μW	1.821μW	0.203mW
Delay	0ns	0.01ns	0.004ns
Max I_{dd} current	0.327mA	0.169mA	0.734mA
Frequency	0.25GHz	0.167GHz	0.25GHz

It is seen that the sleep technique has the moderate power with high speed whereas the PTL logic has lower power consumption but the speed is lower comparatively. In dynamic logic, the power consumption is the maximum. The required current is least in the case of PTL logic.

V. Simulation Results

A graph is drawn between capacitor voltage and power dissipation for the circuits of dual stack with PTL logic, dynamic logic and sleep technique.

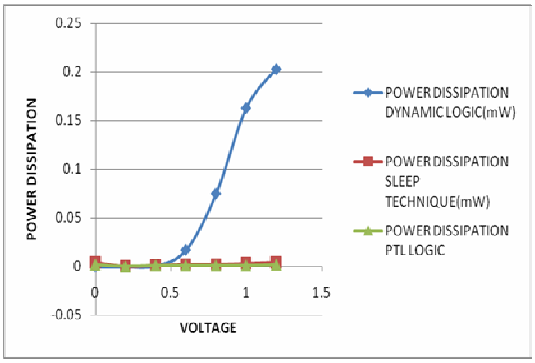

Figure 6. Voltage vs power dissipation.

A graph is drawn between capacitance and final voltage for the circuits and it is seen that for circuit of sleep technique it is exponentially increasing. The same continues to be true at slightly higher value for the circuit of dynamic logic and for PTL logic at a lower value.

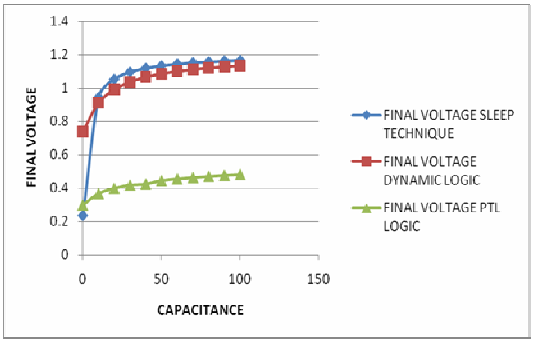

Figure 7. Capacitance vs final voltage.

The values of capacitance versus maximum I_{dd} current and capacitance versus temperature dissipation are also studied. Dual stack with PTL logic shows steady and constant values.

VI. Conclusion

Sub-threshold leakage current in power dissipation is of great challenge in nano meter CMOS technology. The proposed circuit of dual stack with sleep transistor in PTL logic is the new idea for designers in terms of power consumption. The dual stack sleep techniques with different logics are compared. It is found that for a lesser power of PTL logic, the speed gets decreased whereas for other two techniques speed increases for more power. Hence, by adding the sleep transistor to the PTL logic, the speed increases whereas the power consumption decreases.

VII. Future Implementations

Building the dual stack circuit by adding the sleep transistor and PTL logic will increase the speed and decrease the power consumption. These kinds of circuits are advisable for larger architectures with great speed and low power.

Acknowledgement

The authors thank the anonymous referees for their valuable suggestions which let to the improvement of the manuscript.

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