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ACTIVE PARALLEL-RESISTOR-INDUCTOR WITH ELECTRONIC CONTROLLABILITY FOR ANALOG SIGNAL PROCESSING

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Abstract

An active parallel-resistor-inductor using single active element, namely, voltage differencing differential difference amplifier (VDDDA) is proposed in this paper. For this purpose, the resistance and inductance values can be electronically tuned by adjusting bias current of VDDDA. With this feature, the proposed active parallel-RL is attractive to apply in modern electronic devices. The proposed circuit consists of one VDDDA, one resistor and one grounded capacitor. The performance of the proposed active parallel-RL is simulated by PSpice using parameters of 0.18μm TSMC CMOS technology. The simulated results agree well to theoretical anticipation. In particular, the application example as voltage-mode second order high-pass filter using proposed parallel-RL is included to show its usability.

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I. Introduction

The physical coil or inductor is very important in electrical and electronic engineering. It is frequently applied in many applications, especially in analog filter. However, the design of electronic circuit using physical coil has been still had the following drawbacks, the usage of space, weight, cost and tunability [1]. Therefore, the use of active inductor (or called as inductance simulator) to design the signal processing circuit is the excellent way. Mostly, the active inductor constructs from active element and capacitor. Recently, the design of analog circuit using active building block has been more popular than discrete transistor, because it provides the flexibility for designer to implement the circuit with minimum number of active and passive elements [2-6]. In particular, the electronically controllable active building blocks are attractive to synthesis the modern electronic circuits. From literature survey, it is found that inductance simulator using different type of active building blocks can be found, for instance, in [7-22]. However, these proposed inductance simulators so far suffer from the following disadvantages:

- There is non-grounded capacitor, which makes the integration of the active inductor difficult [11-14, 17-19].
- They require passive element matching condition [11, 12, 17, 18, 20].
- They do not exhibit electronic controllability [7, 9-12, 14-18].
- They excessively use number of active and/or passive elements [7-16, 18-20].
- The capacitor is connected to inappropriate terminal of active element, which results in an extra pole, and consequently, lower frequency of operation [21, 22].

The aim of this paper is to propose a grounded parallel-RL simulators using single voltage differencing differential difference amplifier (VDDDA) [23] as active element. The simulated resistance and inductance values can be controlled electronically by adjusting the bias current of the VDDDA. The

proposed simulator comprises one VDDDA, one resistor and one grounded capacitor. The circuit performances are depicted through PSpice simulation, they show good agreement to theoretical anticipation. An application as second-order high-pass filter is included to confirm the usability of proposed circuit.

II. Proposed Circuit

A. Voltage differencing differential difference amplifier (VDDDA)

The principle of VDDDA was introduced in [23]. Its symbol and equivalent circuit are, respectively, shown in Figure 1 and Figure 2, where v+ and v– are the voltage input terminals. The voltage is converted to the *z*-terminal current via a transconductance g_m, which can be tuned by the external bias current. The differential difference of voltages $V_z - V_{vn} + V_{vp}$ is copied to the *w* terminal with the differential-input unity gain buffer. An ideal VDDDA has low-impedance *w* terminal and high-impedance v_+, v_-, *z*, v_n and v_p terminals. The characteristics of VDDDA can be described as follows:

$$\begin{pmatrix} I_{v+} \\ I_{v-} \\ I_z \\ I_{vn} \\ I_{vp} \\ V_w \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 1 \end{pmatrix} \begin{pmatrix} V_+ \\ V_- \\ V_z \\ V_{vn} \\ V_{vp} \end{pmatrix}. \quad (1)$$

For CMOS implementation of VDDDA shown in Figure 3, the g_m is given as

$$g_m = \sqrt{\mu_n C_{ox} \frac{W}{L} I_B}, \quad (2)$$

where I_B is an external DC bias current of the VDDDA and is used to control the g_m. μ_n is the effective channel mobility. C_{ox} is the gate oxide capacitance per unit area. *W* is the channel width and *L* is the channel length.

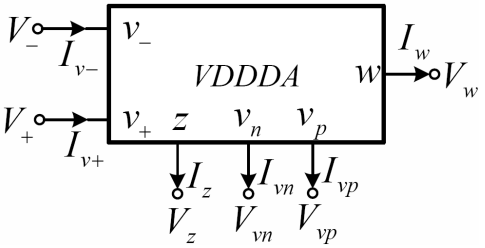

Figure 1. Electrical circuit symbol of VDDDA.

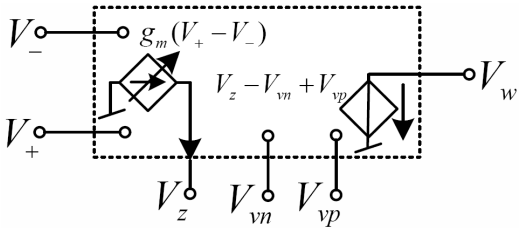

Figure 2. Equivalent circuit of VDDDA.

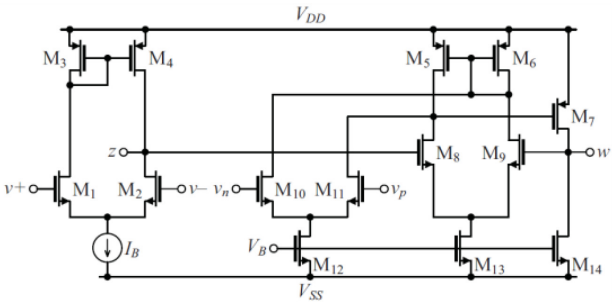

Figure 3. Internal construction of CMOS VDDDA.

B. Proposed active lossy inductance simulator

The proposed circuit realizing grounded active lossy inductance simulator employing single VDDDA, single grounded capacitor, and single resistor is shown in Figure 4. Considering VDDDA properties as described in above, routine analysis of the proposed circuit in Figure 4 gives the following input impedance:

$$Z_{in} = \frac{v_{in}}{i_{in}} = s\frac{RC}{g_m} // \frac{1}{g_m}. \qquad (3)$$

From (3), it is found that the circuit shown in Figure 4 performs a parallel-RL with equivalent resistance R_{eq} and equivalent inductance L_{eq} which are given by

$$R_{eq} = \frac{1}{g_m} \tag{4}$$

and

$$L_{eq} = \frac{CR}{g_m}. \tag{5}$$

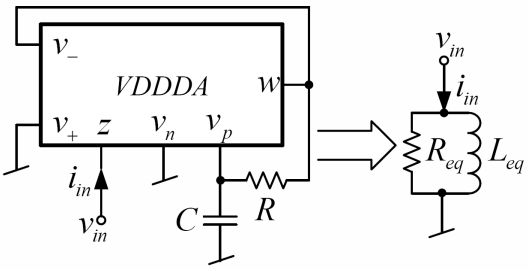

Figure 4. Proposed active lossy inductance simulator.

If g_m is equal to equation (2), then the resistance and inductance values are subsequently modified to

$$R_{eq} = \frac{1}{\sqrt{\mu_n C_{ox} \frac{W}{L} I_B}} \tag{6}$$

and

$$L_{eq} = \frac{CR}{\sqrt{\mu_n C_{ox} \frac{W}{L} I_B}}. \tag{7}$$

It is clearly seen from (6) and (7) that the resistance and inductance values can be adjusted electronically by I_B.

C. Non-ideal analysis

The previous analysis is based on the assumptions that VDDDA has ideal properties. However, in practice implementation, the voltage tracking

errors from the unity-value gain of internal differencing differential difference voltage buffer, and also the parasitic terminal impedances of VDDDA [23] will affect the circuit performance. Taking into account the non-idealities of VDDDA, equation (1) can be modified as

$$\begin{pmatrix} I_{v+} \\ I_{v-} \\ I_z \\ I_{vn} \\ I_{vp} \\ V_w \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \beta_z & -\beta_n & \beta_p \end{pmatrix} \begin{pmatrix} V_+ \\ V_- \\ V_z \\ V_{vn} \\ V_{vp} \end{pmatrix}, \tag{8}$$

where β_z, β_n and β_p represent the voltage error gains from *z*, v_n and v_p terminals to *w* terminal. The influence of parasitic impedances of the v_- terminal of VDDDA is negligible because of their connection to low-impedance outputs *w*. The most important parasitic impedances are resistive and capacitive parts affecting the *z* terminal and v_p terminal, acting in parallel to *C*. Let us denote them R_z, C_z, and R_p, C_p, respectively. Taking them into account together with equation (8), the non-ideal input impedance for the circuit in Figure 4 becomes

$$Z_{in}\left\{ \begin{array}{c} = \dfrac{1}{sC_z} \,//\, R_z \,//\left[\dfrac{(1-\beta_p)}{\beta_z g_m} + \dfrac{s(C+C_p)R}{\beta_z g_m} + \dfrac{R}{\beta_z g_m R_p} \right] // \\ \left[\left(\dfrac{1}{s(C+C_p)} \,//\, R_p \right) \left(\dfrac{1-\beta_p}{\beta_z g_m R} \right) + \dfrac{1}{\beta_z g_m} \right] \end{array} \right\}. \tag{9}$$

III. Simulation Results

Simulation results with PSpice program were carried out to verify appropriate function of the proposed active parallel-RL in Figure 4. Internal construction of VDDDA [23] used in simulation is illustrated in Figure 3. The parameters of PMOS and NMOS transistors are a 0.18μm TSMC CMOS technology. The aspect ratios of PMOS and NMOS transistors are listed

in Table I [23]. The circuit was biased with ±0.9V supply voltages and $V_B = -0.35\text{V}$. The lossy grounded inductance simulator from Figure 4 was designed with the following active and passive element values: bias current $I_B = 50\mu\text{A}$, resistor value $R = 120\Omega$ and capacitor value $C = 47\text{pF}$.

Table I. Dimensions of the MOS transistors

Transistor	W (μm)	L (μm)
M1-2	9	1.08
M3-4	3.96	1.08
M5-7	3.6	1.08
M8-11	0.72	1.08
M12-M14	2.16	1.08

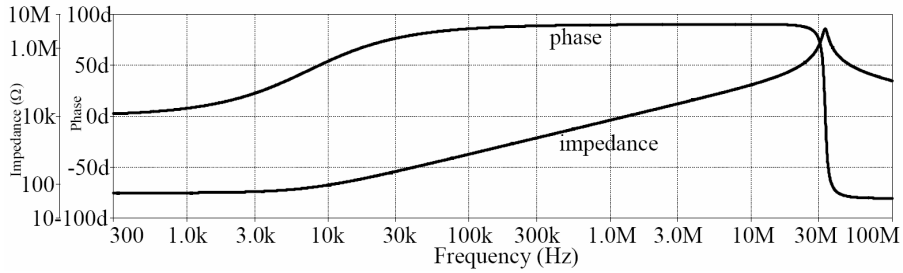

Figure 5. Simulated magnitude and phase responses of the impedance of the proposed lossy inductance simulator shown in Figure 4.

Figure 5 shows the phase and magnitude of input impedance of the circuit in Figure 4. It should be noted that at low and high frequencies, the internal parasitic elements covering capacitances and resistance degrade the performances of the proposed active parallel-RL simulator. Figure 6 shows impedance values with different I_B. It is confirmed that the simulated resistance and inductance values can be adjusted by input bias current as shown in (6) and (7). The total power consumption is about 76.8μW.

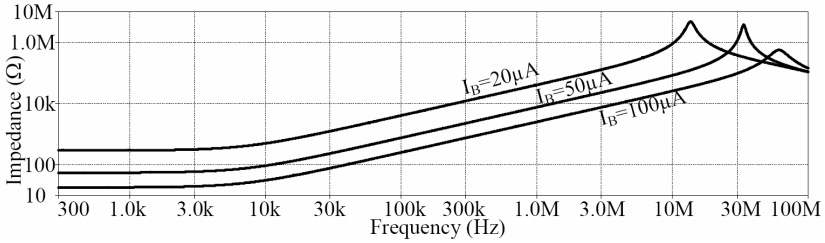

Figure 6. Simulated magnitude responses of the impedance of the proposed lossy inductance simulator shown in Figure 5 for different I_B.

IV. Application Example as 2nd High-pass Filter

In order to show the domain performance of the proposed active inductor in Figure 4, the second-order voltage-mode high-pass filter in Figure 7 was performed. The voltage transfer function is given as:

$$\frac{V_o}{V_{in}} = \frac{s^2}{s^2 + s\left(\frac{1}{R_{eq}C_x} + \frac{1}{L_{eq}C_x}\right)}. \tag{10}$$

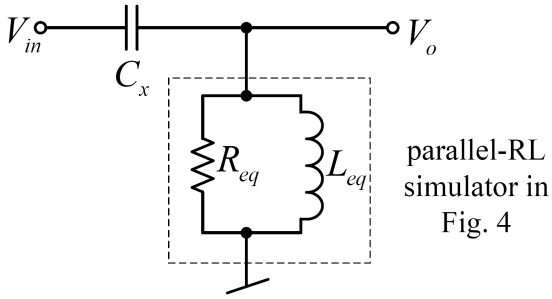

Figure 7. The second-order voltage-mode high-pass filter.

From equation (10), the pole frequency and quality factor are

$$\omega_0 = \frac{1}{\sqrt{L_{eq}C_x}} \tag{11}$$

and

$$Q = R_{eq}\sqrt{\frac{C_x}{L_{eq}}}. \tag{12}$$

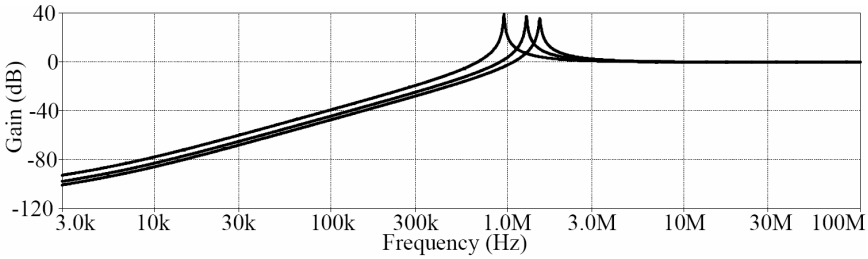

Figure 8. Simulated gain response of the high-pass filter shown in Figure 7 for different I_B.

The filter was verified with I_B = 20μA, 50μA and 100μA, R = 120Ω, C = 100pF and C_x = 100pF. The high-pass responses with different I_B are shown in Figure 8. It is confirmed that the cut-off frequency can be adjusted by equivalent inductance by means of bias current as shown in (7).

V. Conclusion

In this paper, a new active parallel-RL simulator has been presented. The proposed circuit has a simple configuration with single VDDDA, single resistor and single grounded capacitor. The resistance and capacitance values can be electronically tuned. Simulation results are also included to confirm the characteristics of the proposed simulator. Finally, the application example as high-pass filter constructed from proposed active parallel-RL is also implemented to show the usability of the proposed circuit.

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References

[1] A. Thanachayanont and A. Payne, CMOS floating active inductor and its application to bandpass filter and oscillator designs, IEE Proc. -Circuits Device Syst. 147 (2000), 42-48.

[2] D. Biolek, R. Senani, V. Biolkova and Z. Kolka, Active elements for analog signal processing: classification, review, and new proposals, Radioengineering 17(4) (2008), 15-32.

[3] W. Jaikla, D. Biolek, S. Siripongdee and J. Bajer, High input impedance voltage-mode biquad filter using VD-DIBAs, Radioengineering 23(3) (2014), 914-921.

[4] W. Mekhum and W. Jaikla, Resistorless cascadable current-mode filter using CCCFTAS, Advances in Electrical and Electronic Engineering 11(6) (2013), 501-506.

[5] K. Pal, New inductance and capacitor floatation schemes using current conveyors, Electronics Letters 17 (1981), 807-808.

[6] R. Senani, Realization of a class of analog signal processing/signal generation circuits: novel configurations using current feedback op-amps, Frequenz 52(9-10) (1998), 196-206.

[7] V. Singh, Active RC single-resistance-controlled lossless floating inductance simulation using single grounded capacitor, Electronics Letters 17 (1981), 920-921.

[8] M. Higashimura and Y. Fukui, Simulation of lossless floating inductance using two current conveyors and an operational transconductance amplifier, International Journal of Electronics 66 (1989), 633-638.

[9] W. Kiranon and P. Pawarangkoon, Floating inductance simulation based on current conveyors, Electronics Letters 33 (1997), 1748-1749.

[10] P. V. A. Mohan, Grounded capacitor based grounded and floating inductance simulation using current conveyors, Electronics Letters 34(11) (1998), 1037-1038.

[11] H. Kuntman, M. Gulsoy and O. Cicekoglu, Actively simulated grounded lossy inductors using third generation current conveyors, Microelectronics Journal 31(4) (2000), 245-250.

[12] J. S. Pena-Finol and J. A. Connelly, Novel lossless floating immittance simulator employing only two FTFNs, Analog ICs and Signal Processing 29 (2001), 233-235.

[13] I. A. Khan and M. H. Zaidi, A novel ideal floating inductor using translinear conveyors, Active and Passive Electronic Components 26(2) (2003), 87-89.

[14] U. Çam, F. Kaçar, O. Cicekoglu, H. Kuntman and A. Kuntman, Novel grounded parallel immittance simulator topologies employing single OTRA, AEU-International Journal Electronics and Communications 57(4) (2003), 287-290.

[15] G. Ferri, N. C. Guerrini and M. Diqual, CCII-based floating inductance simulator with compensated series resistance, Electronics Letters 39(22) (2003), 97-98.

[16] K. Pal, Floating inductance and FDNR using positive polarity current conveyors, Active and Passive Electronic Components 27 (2004), 81-83.

[17] E. Yuce, S. Minaei and O. Cicekoglu, A novel grounded inductor realization using a minimum number of active and passive components, ETRI Journal 27 (2005), 427-432.

[18] M. Gulsoy and O. Çcekolu, Lossless and lossy synthetic inductors employing single current differencing buffered amplifier, IEICE Transaction on Communications E88-B(5) (2005), 2152-2155.

[19] M. Minaei, E. Yuce and O. Cicekoglu, Lossless active floating inductance simulator, Proceedings of DELTA'06, KL, Malaysia, 2006, pp. 332-335.

[20] C. Koomgaew, W. Petchmaneelumka and V. Riewruja, OTA-based floating inductance simulator, ICROS-SICE International Joint Conference, 2009, pp. 857-860.

[21] D. Siriphot, S. Maneewan and W. Jaikla, Single active element based electronically controllable grounded inductance simulator, 6th Biomedical Engineering International Conference, BMEiCON 2013, Krabi, Thailand, 23 October 2013.

[22] A. Chaichana and W. Jaikla, Electronically tunable inductance simulator for monitoring biomedical signals, International Journal of Bioscience, Biochemistry and Bioinformatics (IJBBB) 4(1) (2014), 45-48.

[23] N. Herencsar, R. Sotner, B. Metin, J. Koton and K. Vrba, VDDDA - new 'voltage differencing' device for analog signal processing, Proceeding of the 8th International Conference on Electrical and Electronics Engineering, Bursa, Turkey, The Chamber of Electrical Engineers Bursa Branch (EMO), 2013, pp. 17-20.