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PLL ENERGY CONSUMPTION MODEL, OPTIMIZATION AND DESIGN METHOD FOR A VERY LOW POWER APPLICATION

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Abstract

We present typical theoretical power consumption model of the PLL system in this paper. We have based our study on the most general used PLL elements. Optimization and the design technique for better power transfer between circuit elements and therefore, better power transfer efficiency has been outline for power expenditure minimization.

Keywords and phrases : power supply, PLL, low power application, MOS integrated circuits, energy efficiency, wireless system.

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1. Introduction

Within a general framework, the applications based on the electric power are in perpetual growths because of their impact on modernization. For as much reliability, the energy efficiency and the effectiveness of the electric systems must continuously be improved in order to minimize the consumption of the electric power which is more and more appraisal.

The Phase Locked Loop (PLL) is largely used in the communication systems such as wireless systems, where the desire for portability of electronic equipment generated a need for low power systems with the battery operated products like hearing aids, implantable cardiac pacemakers, cell phones and hand held multimedia terminals. Low power dissipation is attractive, and perhaps even essential in these applications to have reasonable battery life and weight. The ultimate goal in design is close to have battery-less systems, because the battery contributes greatly to volume and weight.

These wireless systems architectures are often projected according to components immediately available, the integrated circuits intended to be used as much as architectures than possible lead too much system redundancy. This increases the requirement in energy for these systems and generally affects their performances. For a multidisciplinary of these integrated circuits, a close cooperation between the academicians and industries of manufacture is essential [21].

The various parameters [13] implied in the design of wireless elements systems and thus, of the PLL are recapitulated in Figure 1; the consumption, that is the energy necessary, is severely constrained by the seven illustrated parameters. It should be noted that in general, wireless circuits cannot profit as much from advanced technological circuit integration as well as the numerical systems; this is due to the fact that wireless systems require components such as inductances and capacities for examples, whose integration always has a certain delicacy in spite of the technological projections.

In the following, we will first present and define the various types of energy consumption in an electronic circuit in general, and in particular in a PLL circuit; their mathematical models will be elaborated starting from the basic components models energy consumption relative with the parameters of Figure 1. We will secondly derive a global consumption model of a PLL. In the third and last part, an

optimization outline and a better efficiency design method for supply power minimization are presented.

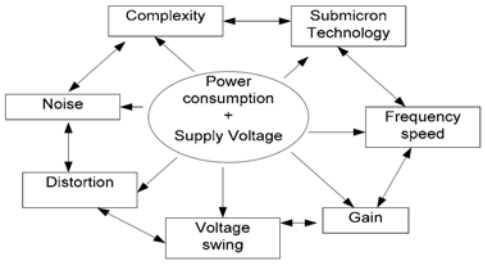

Figure 1. Power supply parameters in wireless systems design.

2. Energy Consumption Types in an Electronic Circuit

An active electronic circuit needs as a preliminary an external polarization energy contribution for fulfilling the function for which it is conceived. This contribution is one of the sources of energy expenditure in an electronic circuit and is described as static. In addition to the polarization current, short circuit current, leakage and conduction current (during states transitions) generate major energy (running, biasing and by Joule effect energy) expenditure. In third position, the energy losses from the capacitor and parasitic capacitor of the circuit; indeed, the charge and discharges of the various nodes capacities of the circuit could not be done without energy escapes; this loss is described as dynamics. The fourth and last source of energy dissipation is the internal noise which generates also considerable losses.

3. Sources and Expenditure of Energy in a PLL Circuit

A. PLL circuit description

A PLL system is a physical device which reproduces at the output, the excitation signal at the input with the phase image at least or the same phase at best. We have in Figure 2 an example of a block diagram of a PLL system; for our typical study, we choose for each of the PLL fundamental elements, the most used structure such as phase-frequency comparator with charge pump (PFC-CP), the low pass filter (LPF), a LC voltage controlled oscillator (LC-VCO) and a counter as frequency divider (FD).

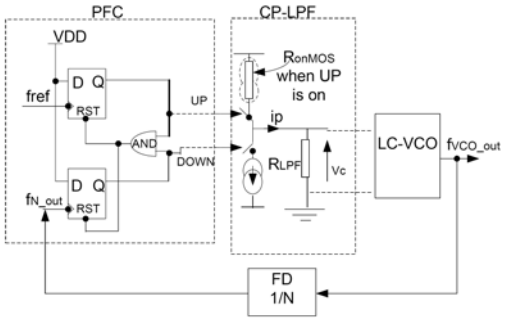

Figure 2. Typical PLL circuit block.

B. Noise, definition and power supply model in a CP circuit

In a PLL system, a noise can be thermal 1/f, and of phase; we do not consider in our work the external noise source which is out of our control. In charge pump (CP) PLL, the PFC outputs up and down, produce narrow pulse in each phase comparison period T_{ref}, the CP generates the corresponding charge pump output current.

Noises in PLL generate the random part of the charge pump output current. The noise associated with each PLL block and mainly from the input or reference frequency, through their transfer function, can produce phase error noise $\delta\theta_e$ (known as jitter in time domain) at the PFC output. Figure 3 illustrates the probably charge pump current impulse sequences due to the phase error noise.

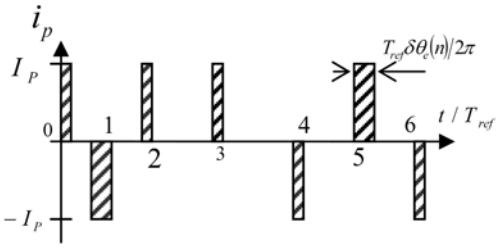

Figure 3. Charge pump output sequences current in locked state due to noise.

According to the fact, that PFC-CP operate in discrete-time manner, the spectrum of the discrete time phase error is that of the continuous time $\delta\theta_e$ repeated in the frequency domain with period equal to the reference frequency ω_{ref},

$$\delta\theta_{e\_dt}(\omega) = \sum_{n=-\infty}^{n=+\infty} \delta\theta_e(\omega + n\omega_{ref}). \quad (1)$$

That is the spectrum folding effect due to sampling effect produces phase noise around offset frequencies of $n\omega_{ref}$, where $n = \pm 1, \pm 2, \pm 3, ...,$ this phase noise around offset frequencies $\pm\omega_{ref}$ is accounted for the reference spur, the corresponding leakage current in CP is given by (2),

$$i_{p\_dt}(\omega) = \frac{I_{CP}}{2\pi}\delta\theta_{e\_dt}(\omega). \tag{2}$$

For this current from (2), the corresponding power supply model of (3) is the sum of static power supply and the thermal power supply (due to the current leakage flow in the CP conduction resistance and the LPF resistance),

$$P_1 = (R_{onMOS} + R_{LPF}) \cdot |i_{p\_dt}(\omega)|^2 + V_{DD}|i_{p\_dt}(\omega)|, \tag{3}$$

where R_{onMOS} and R_{LPF} are, respectively, the CP CMOS transistor resistance in up or down on state and LPF equivalent resistance.

The thermal CP current noise can be represented by (4) [27], where t_{on} is the turn-on time of the CP, V_{od_CP} is the gate-to-source overdrive voltage $(V_{GS}\text{-}V_T)$ of the current source or sink transistor in the CP, *K* is the Boltzman constant and *T* is the temperature,

$$i^2_{CP\_th}(\omega) = 2\frac{t_{on}}{T_{ref}} \cdot 4KT \cdot \frac{2I_P}{V_{od\_CP}}. \tag{4}$$

As in (3), the corresponding power supply model is given by (5),

$$P_2(\omega) = (R_{onMOS} + R_{LPF}) \cdot i^2_{CP\_th}(\omega) + V_{DD}|i_{CP\_th}(\omega)|. \tag{5}$$

C. Technology and power supply model in CP and LPF circuit

The power dissipation in an electronic circuit depends on many considerations, majority of them is related on the limitations and the complexity of technology employed.

In the PLL modern circuits, where the leakage currents are not any more that about the nano Ampere and not consequently constituting the dominant source of losses, it is important to take into account all the other factors contributing to the losses.

In CP circuit, the leakage current, the mismatch current and the timing mismatch current, are a current loses relative to the technology used; mismatches generate deterministic and periodic ripples of the VCO control voltage. Indeed, the difference between the CMOS transistors of the CP and the imperfection of the circuits correcting the dead zone of CP prevent perfect symmetry between the current injected and withdrawn of the loads of the filter. This dissymmetry (mismatch) [23] can increase the operating time (by a term of timing mismatch) of the PFC CP and involves parasitic impulse peaks (Pulse Spur), it can also appear by the inequality of the discharge and charging currents (current mismatch) [23].

Since the CP output current is a periodic signal with period of T_{ref}, it can be decomposed into discrete Fourier series as given by (6) [22],

$$i_p(t) = \sum_{k=1}^{\infty} C_k e^{jk\,\omega_{ref} t}. \tag{6}$$

Figure 4 shows the CP output current due to the timing mismatch between the turn off, of up and down switches.

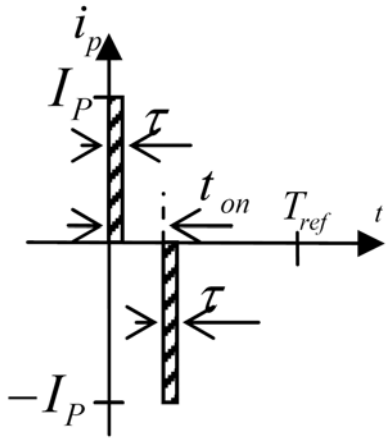

Figure 4. Timing mismatch.

It might be due to the delay mismatch between falling edges of up and down, or the turn off time mismatch between the two switches themselves. It generates both positive and negative current pulses of the same width [14]. We denote by τ the current pulse width to compensate the time mismatch current.

According to Figure 4, we derive the Fourier coefficients of (7),

$$C_k\,|_{t\_mismatch} = \frac{1}{T_{ref}}\left[\int_0^{\tau} I_P e^{-jk\omega_{ref}t}dt - \int_{t_{on}}^{t_{on}+\tau} I_P e^{-jk\omega_{ref}t}dt\right]. \tag{7}$$

If we neglect the other harmonics contribution compared to the reference spur, then we obtain (8) from (7),

$$i_p(t)|_{t\_mismatch} \approx |C_1|_{t\_mismatch}| \approx 2\pi I_P \frac{\tau}{T_{ref}} \cdot \frac{t_{on}}{T_{ref}}. \tag{8}$$

The corresponding supply power model is derived by (9),

$$P_3(\omega) = (R_{onMOS} + R_{LPF}) \cdot \left(2\pi I_P \frac{\tau}{T_{ref}} \cdot \frac{t_{on}}{T_{ref}}\right)^2 + 2\pi I_P \frac{\tau}{T_{ref}} \cdot \frac{t_{on}}{T_{ref}} V_{DD}. \tag{9}$$

Figure 5 presents the current mismatch ΔI_P between the up I_{P_up} and down I_{P_dn} currents, τ specified by (11) is the current pulse width of the sinking current to compensate the current mismatch,

$$\Delta I_P = I_{P\_up} - I_{P\_dn}, \tag{10}$$

$$\tau = \frac{\Delta I_P}{I_P} t_{on}. \tag{11}$$

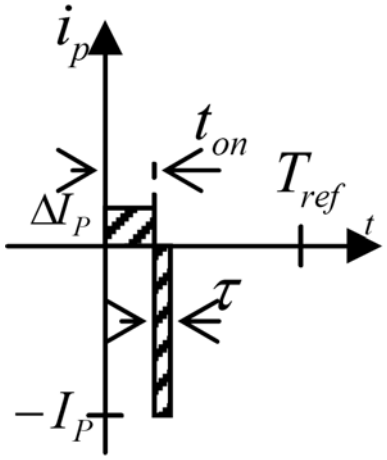

Figure 5. Current mismatch ΔI_P.

The corresponding Fourier coefficients of the CP output current are specified by (12),

$$C_k|_{c\_mismatch} = \frac{1}{T_{ref}}\left[\int_0^{t_{on}} \Delta I_P e^{-jk\omega_{ref}t}dt - \int_{t_{on}}^{t_{on}+\tau} I_{fuite} e^{-jk\omega_{ref}t}dt\right]. \quad (12)$$

We suppose $\Delta I_P << I_P$, and $t_{on} << T_{ref}$, if we neglect the other harmonics contribution compared to the reference spur, (6) and (12) yield to obtain (13),

$$|i_p(t)|_{c\_mismatch}| = C_1|_{c\_mismatch} \approx \pi\Delta I_P\left(\frac{t_{on}}{T_{ref}}\right)^2. \quad (13)$$

The corresponding supply power model is derived by (14),

$$P_4(\omega) = (R_{onMOS} + R_{LPF}) \cdot \left[\pi\Delta I_P\left(\frac{t_{on}}{T_{ref}}\right)^2\right]^2 + V_{DD}\pi\Delta I_P\left(\frac{t_{on}}{T_{ref}}\right)^2. \quad (14)$$

For the leakage current compensation, Figure 6 illustrates the corresponding pulse width τ which expression is specified by (15),

$$\tau = \frac{I_{leak}}{I_P} T_{ref}. \quad (15)$$

The corresponding Fourier coefficients of the CP output current are specified by (16),

$$C_k|_{leak} = \frac{1}{T_{ref}}\left[\int_0^{\tau} I_P e^{jk\omega_{ref}t}dt + \int_0^{T_{ref}} I_{fuite} e^{jk\omega_{ref}t}dt\right]. \quad (16)$$

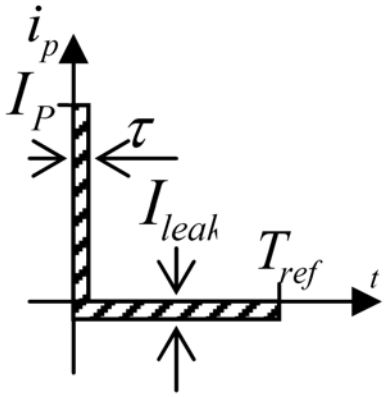

Figure 6. Leakage current.

Since $I_{leak} << I_P$, we have $\tau << T_{ref}$, this consideration yields at a Fourier coefficient (17) and a corresponding CP output leakage current (18) for the reference spur,

$$| C_1 | \approx I_{leak}, \tag{17}$$

$$i_p(t)|_{fuite} = | C_1 | = I_{leak}. \tag{18}$$

The corresponding supply power model is derived by (19),

$$P_5(\omega) = I_{leak}^2 \cdot (R_{onMOS} + R_{LPF}) + I_{leak} V_{DD}. \tag{19}$$

D. Technology and power supply model in FD and PFC circuit

The FD and the PFC are logic integrated circuits. The increasing request in wireless telecommunications systems made evolve a very large scale integration (VLSI) technology; the batteries technology not being able to go at the rhythm of VLSI, we are thus, limited by the power density. It is, then necessary to face the challenges such as very low power consumption, very high frequencies and very small integration surface. One of the solutions is the low voltage devices, which is unfortunately confronted with the noise level and the threshold voltage of the elementary components used.

To control these multiple constraints, we have in the literature the components and CMOS logic circuits design techniques for very low energy consumption, we have in particular MOSFETs working under the threshold voltage [25, 24], substrate controlled transistors [25, 24, 19, 16], floating gate approaches structures [25, 20, 12]. The ultra low voltage (ULV) logic gate construct with floating gate approach structures, studied and tested in a 0.13μm process for operating voltage of 0.4V [3], is built around a CMOS structure with floating gate. This configuration thus, leaves the possibility of modifying the threshold voltage of operation circuit. One of the major assets of the ultra low voltage gate structure is short circuit current elimination during the transitions. The simple design of an ultra low voltage gate consisted of make small changes to the traditional CMOS gate [3].

We have in general four power supply sources in a basic CMOS circuit, dynamic (capacitor charge and discharge), static (running and biasing), thermal (by Joule effect) and of short-circuit (during the simultaneous conduction instant of the CMOS circuit transistors). In the logic gate system, more than 90% of the power consumption takes place during transitions between states [5]. For global power

supply evaluation in each integrated circuit, let us suppose that it is structured by various elementary functional structures with an input impedance capacitor C (gate capacitor in general) and a conduction resistance R_{on} as shows in Figure 7. Thus, the input capacitor of each elementary circuit is the load of another one. Hence, the global integrated logic circuit can be modeled by a MOSFET structure.

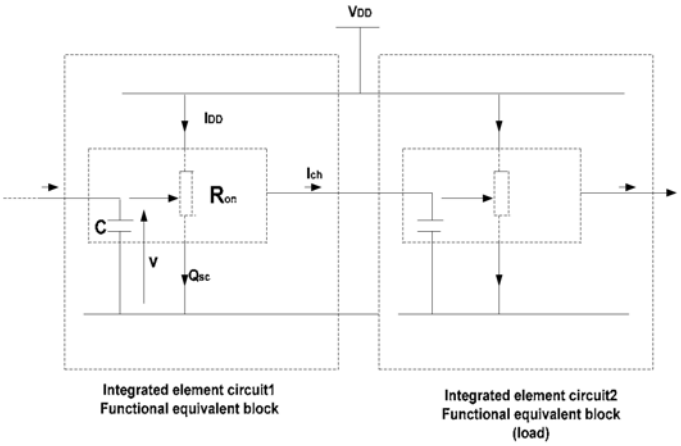

Figure 7. Integrated circuit equivalent functional block.

The basic power supply for a CMOS circuit is evaluated by (20) [1, 2],

$$P_{IC}(\omega) = \beta CVfV_{DD} + \beta Q_{SC}V_{DD}f + I_{DD}V_{DD} + \beta R_{on}I_{DD}^2, \tag{20}$$

where β is the commutation activity (number of transitions per cycle), I_{DD} is the average current supply during the circuit element time on, f is the operating frequency, Q_{SC} is the charge lost due to the short-circuit current towards the mass at each commutation, C is total capacitor at the various nodes of commutations, R_{on} is the total resistance of the circuit element during conduction instant.

According to (20), we derive at (21) the supply power model of the FD circuit. Notice that in our integrated circuit power supply evaluation, we suppose the use of ULV technology, i.e., the charge lost due to the short-circuit current towards the mass will be neglected,

$$\begin{aligned} P_N(\omega) &= \beta C_N V f_{in\_N} V_{DD} + I_{DD\_N}V_{DD} + \beta R_{onN} I_{DD\_N}^2 \\ &= I_{DD\_N}V_{DD} + \beta C_N V N f_{in\_N} V_{DD} + \beta R_{onN} I_{DD\_N}^2, \end{aligned} \tag{21}$$

where f_{in_N} and f_{out_N} are, respectively, the FD input and output signal frequency, N is the FD divider ratio, R_{onN} is the global FD conduction resistance at each commutation activity β, C_N is FD total capacitor at the various nodes of commutations and I_{DD_N} is the average current supply during the circuit element time on of the FD.

The PFC block is made with one logic AND gate and two edge-triggered D flip-flop. From (20), we derive at (22) the PFC power supply,

$$P_{PFC}(\omega) = V_{DD}I_{DD\_A} + \beta R_{onA}I_{DD\_A}^2 + \beta C_A V(\delta\theta_e + \Delta f)V_{DD} + \beta C_D V(f_{ref} + f_{out\_N} + 2\Delta f)V_{DD} + V_{DD}I_{DD\_D} + \beta R_{onD}I_{DD\_D}^2, \quad (22)$$

where R_{onA} and R_{onD} are, respectively, the AND gate and edge-triggered D flip-flop global conduction resistance, C_D and C_A are the total capacitor at the various nodes of commutations of the AND gate and edge-triggered D flip-flop, respectively, I_{DD_A} and I_{DD_D} are, respectively, the average current supply during the circuit element time on of the AND gate and edge-triggered D flip-flop.

E. Technology and power supply model in a LC-VCO circuit

The low voltage levels in the analogical electronics devices guarantee their effectiveness and reduce also considerably the energy level necessary for their operation. The first aiming strategic of the analogical circuit's design is often the high speed (frequency) and dynamic broad band, one of the factors directly affected by this aiming is the spectral purity and therefore, the power dissipated in the circuit. It is thus, essential to locate the responsible elements and to minimize them within the possible limit.

For the LC-VCO power supply evaluation, we have chosen the Colpitts oscillator circuit of Figure 8, below.

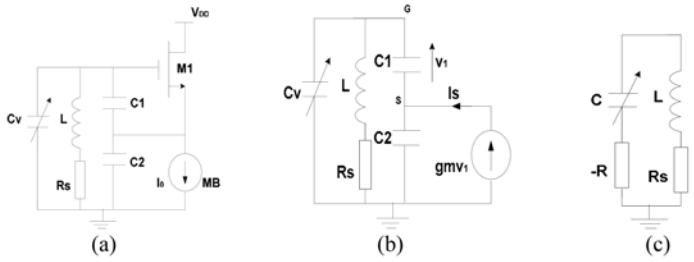

Figure 8. LC-VCO simplified Colpitts circuit representation.

We have in Figure 8(a) a typical representation of Colpitts oscillator, in Figure 8(b) an equivalent circuit with the transistor represented by a linear transconductance gm for small signals, in Figure 8(c) an equivalent negative resistance model of oscillator.

The oscillation frequency is tuned by a varactor structure of Cv equivalent capacitor composed by NMOS transistors running in inversion mode capacitance. All the resistive losses of the tank have been lumped into a single resistor Rs.

During start-up, the average current in transistors may not be the same as the bias current; the average current will change in the direction of the bias current. For the LC-VCO current supply, we will assume first that in the steady-state oscillation, gate-source amplitude *Vm* and gate DC bias *Vb* for M1's transistor are bound by two constraints for a high quality factor of the passive tank, so that the AC gate voltage *Vgs* (*t*) is practically a pure sine wave [13]; hence, transistor M1 can be described by (23), where *VT* is the threshold voltage,

$$I_{DS}(t) = \frac{\lambda}{2}[V_{gs}(t) + Vb - VT]^2, \tag{23}$$

where λ is the transistor geometric parameter and $V_{gs}(t) = Vm\cos(\omega t)$.

This assumption, i.e., the drain source current harmonics sufficiently filtered by the tank, lead to the calculation in (25) of the fundamental harmonics average supply current I_0, through M1, we assume that *Vb*-*VT* is greater than *Vm* for avoid the transistor cut off,

$$I_0 = \frac{1}{T}\int_0^T \frac{\lambda}{2}[Vm\cos(\omega t) + Vb - VT]^2 dt \tag{24}$$

$$= \frac{\lambda Vm^2}{4}[1 + 2x^2], \tag{25}$$

where $x = (Vb - VT)/Vm$ is a defining constant; the amplitude limit is $Vm = 2I_0/gm$ [13, 18].

Above, we assume for the fundamental harmonics current supply I_0 that the AC gate voltage *Vgs* (*t*) is practically a pure sine wave; this assumption is not true in practice. Indeed, the harmonics gate voltage, generally named phase noise will generate the drain noise current. Experimentally, the qualitative behaviour of phase

noise has been well known. An oscillator's output power spectrum consists of a peak at the carrier frequency surrounded by a noise skirt symmetrical to the carrier frequency. This noise manifests itself in the time domain as jitter around the oscillation's zero-crossing points. Oscillator noise is therefore, usually referred to as phase noise. The assumption of phase noise implies that the sideband spectrum above and below the carrier frequency must be equal in amplitude and opposite in sign.

The phase noise impact oscillator in RF and other communication circuits has made it one of the most extensively studied subjects in electronics. Journal papers on the subject [11, 8, 9, 15, 10, 26 and 28] can be found. The too numerous papers on LC oscillators serve to underline the fact that existing theories on phase noise have not been universally found satisfactory. Hence, we will consider secondly for a LC-VCO main transistor M1 drain noise current supply I_{0n}, an interfering gate source harmonics voltages at both frequencies $\omega + \Delta\omega$ and $\omega - \Delta\omega$. So, the corresponding interfering M1 gate voltage can be described by (26),

$$V_{ings}(t) = V_1 \cos[(\omega + \Delta\omega)t] + V_2 \cos[(\omega - \Delta\omega)t]. \tag{26}$$

The total AC drain current supply in steady state is therefore,

$$I_{TDS}(t) = \frac{\lambda}{2}\begin{bmatrix} V_{gs}(t) + V_1 \cos[(\omega + \Delta\omega)t] \\ \\ + V_2 \cos[(\omega - \Delta\omega)t] + Vb - VT \end{bmatrix}^2. \tag{27}$$

The average total current supply I_{T0} through M1 is evaluated by

$$I_{TO} = \frac{\lambda}{2T}\int_0^T \begin{bmatrix} V_{gs}(t) + V_1 \cos[(\omega + \Delta\omega)t] \\ \\ + V_2 \cos[(\omega - \Delta\omega)t] + Vb - VT \end{bmatrix}^2 dt$$

$$= \frac{\lambda}{2T}\int_0^T [V_{gs}(t) + Vb - VT]^2 dt$$

$$+ \frac{\lambda}{2T}\int_0^T \begin{Bmatrix} [V_1 \cos(\omega + \Delta\omega)t + V_2 \cos(\omega - \Delta\omega)t] \\ \\ + 2[V_1 \cos(\omega + \Delta\omega)t + V_2 \cos(\omega - \Delta\omega)t][V_{gs}(t) + Vb - VT] \end{Bmatrix}^2 dt$$

$$= I_O + I_{nO},$$

where

$$I_{nO} = \frac{\lambda}{2T}\int_0^T \left\{ \begin{array}{l} [V_1 \cos(\omega + \Delta\omega)t + V_2 \cos(\omega - \Delta\omega)t] \\ + 2[V_1 \cos(\omega + \Delta\omega)t + V_2 \cos(\omega - \Delta\omega)t][V_{gs}(t) + Vb - VT] \end{array} \right\}^2 dt.$$

If we assume that the harmonics of frequency 2ω will be filtered by the tank, then we obtain a noise current expression given by (28),

$$I_{nO} = \frac{\lambda}{2\Delta\omega}\left[V_1V_2 + 2(V_2V_m + V_1V_m) + (Vb - V_T)\left(\frac{\Delta\omega V_2}{\omega + \Delta\omega} - \frac{\Delta\omega V_1}{\omega - \Delta\omega}\right)\right]\sin\frac{\Delta\omega}{f}. \quad (28)$$

If we take in account the assumption that the sideband spectrum above and below the carrier frequency must be equal in amplitude and opposite in sign, at suppose also that $\omega >> \Delta\omega$, (29) yields to

$$I_{nO} = \frac{\lambda V_m^2}{2\Delta\omega}[1 + 4\zeta]\sin\frac{\Delta\omega}{f} \quad (29)$$

with $\zeta = V_1/V_m$, a defining noise constant.

In addition to the average fundamental harmonics current supply I_0 and the phase noise current supply I_{0n}, we have at different LC-VCO branch the corresponding thermal noise current supply [13] as presented in Figure 9. All major noise sources have been identified and convert into equivalent supply current in the oscillator, i.e., the thermal noise current associated with the bias transistor MB, the thermal noise current due to the loss resistance of the tank Rs, and the thermal noise current due to the main switching transistor M1.

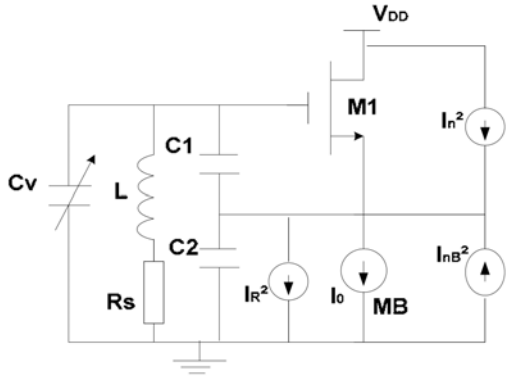

Figure 9. Colpitts oscillator with all thermal noise sources represented as current.

The total corresponding thermal noise current is defined, respectively, by (30), (31) and (32) [13],

$$I_{nB}^2 = \frac{8kT}{3} gmB, \tag{30}$$

$$I_R^2 = 4kTRs \cdot (\omega C_2)^2, \tag{31}$$

$$I_n^2 = \frac{8kT}{3} gm0 \sqrt{\frac{\cos^{-1}(x)}{\pi}}, \tag{32}$$

where $gm0 = \sqrt{2\lambda I_0}$ is a $M1$ nominal transconductance and gmB is the MB transconductance.

The main switching transistor also supply current for the charge and discharge of the gate parasitic capacitor C_{gM1}, this current can be defined by (33) according to (20),

$$I_{gM1}(\omega) = fC_{gM1}Vb. \tag{33}$$

Therefore, the total supply current in the LC-VCO Colpitts oscillator is simply the sum of the average current I_0 and the total supply noise current,

$$\begin{aligned} I_{VCO}(\omega) = {} & \frac{\lambda Vm^2}{4}[1 + 2x^2] + \sqrt{\frac{8kT}{3} gmB} \\ & + 2\omega C_2 \sqrt{kTRs} + \sqrt{\frac{8kT}{3} gm0 \sqrt{\frac{\cos^{-1}(x)}{\pi}}} + fC_{gM1}Vb \\ & + \frac{\lambda V_m^2}{2\Delta\omega}[1 + 4\zeta]\sin\frac{\Delta\omega}{f}. \end{aligned} \tag{34}$$

Therefore, the corresponding LC-VCO power supply is subsequently derived at (35),

$$P_{VCO}(\omega) = \left\{ \begin{array}{l} \dfrac{\lambda Vm^2}{4}[1 + 2x^2] + \sqrt{\dfrac{8kT}{3} gmB} + fC_{gM1}Vb \\ + 2\omega C_2 \sqrt{kTRs} + \sqrt{\dfrac{8kT}{3} gm0 \sqrt{\dfrac{\cos^{-1}(x)}{\pi}}} \\ + \dfrac{\lambda V_m^2}{2\Delta\omega}[1 + 4\zeta]\sin\dfrac{\Delta\omega}{f} \end{array} \right\} V_{DD}. \tag{35}$$

F. Power supply model in a PLL circuit

This PLL power supply model is simply the sum of the giving PLL blocks elements power supply defining by P_N, $P_{CP\text{-}LPF}$, P_{PFC} and P_{VCO},

$$P_{PLL}(\omega) = P_{CP-LPF}(\omega) + P_N(\omega) + P_{PFC}(\omega) + P_{VCO}(\omega), \tag{36}$$

where $P_{CP\text{-}LPF}$ is the charge pump and low pass filter power supply defining by the expression below,

$$P_{CP-LPF}(\omega) = P_1(\omega) + P_2(\omega) + P_3(\omega) + P_4(\omega) + P_5(\omega)$$

with P_1, P_2, P_3, P_4 and P_5 the above defining different power supply.

4. A PLL Circuit Power Supply, Optimization

During transistors conduction instance, i.e., circuit in transition states, approximately the 90% of the losses of energy are operated [5]. A rather low response time and low conductions resistances are effective means able to guarantee an attenuation of this large energy expenditure. These conductions resistances and transition times are functions of the geometrical parameters of the transistors. It would be thus, interested to find an area of agreement between the effectiveness and the low energy expenditure by an optimization of the geometrical parameters.

For this optimization, we have chosen the total power loss in simple CMOS element circuit operating in a commutation mode as usually in more integrated circuit, it can also be applied to a simple MOS for main switching transistor as M1.

According to the different power supply types described before, we derive the total power of this CMOS circuit in (37) below,

$$P_{global} = f(C_L + C_{gn} + C_{gp})V^2 + \beta \cdot I_D^2[xR_{on,p} + R_{on,n}(1-x)] + I_{stat}V_{DD} \tag{37}$$

with $C_L = C_g(w_p + w_n)$, $C_{gp} = w_p(C_{ox}\ell + 2C_0)$ and $C_{gn} = w_n(C_{ox}\ell + 2C_0)$ [17].

Here I_D is the average supply current during each elementary conduction time interval, C_g is the gate capacitor per unit of width deduced from the manufacturing process parameters, C_{gp} and C_{gn} are the gate capacitors of the PMOS and NMOS, respectively, C_{ox} and C_0 are the process parameters, x is the ratio of the CMOS circuit conduction time to the PMOS conduction time, and $R_{on,n}$ is the NMOS

conduction resistance defining by (38), the same expression can be derived for the PMOS conduction resistance $R_{on,\,p}$ with the simple substitution of w_n and k_n by w_p and k_p,

$$R_{on,\,n} = \frac{\ell}{k_n w_n V_{GT}}. \tag{38}$$

According to (38), we can obtain very low resistance values for high w_n values. However, the gate capacitor and the response time will increase with w_n. An optimum must be found; the w_n optimum value not only minimizes total losses, but also maintains a good response time of CMOS transistors. So, it is very important to find good ratios between the losses of power, w_n and w_p. The essential variables in the global power defining at (37) are w_n and w_p. In the CMOS structure, condition (39) [6] is necessary for the NMOS and PMOS equal response time; the consider ratio δ between the PMOS and NMOS transistor width is because of their mobility charge difference. The optimum expressions of w_n and w_p will be obtained by solving (40) below,

$$\delta = \frac{w_p}{w_n} = \sqrt{\frac{k_n}{|k_p|}} = \frac{1}{\gamma} \tag{39}$$

with $\gamma = \dfrac{R_{on,\,p}}{R_{on,\,n}}$

$$\left[\frac{d(P_{globale})}{dw_n}\right]_{w_p = cste} = 0 \quad \text{and} \quad \left[\frac{d(P_{globale})}{dw_p}\right]_{w_n = cste} = 0. \tag{40}$$

The resolution of (40) yields to the optimum geometric parameters $w_{n,\,opt}$ and $w_{p,\,opt}$ below,

$$w_{n,\,opt} = \frac{I_D}{V}\sqrt{\frac{l\beta(1-x)}{k_n V_{GT} f[C_g + (C_{ox} l + 2C_0)]}}, \tag{41}$$

$$w_{p,\,opt} = \delta\frac{I_D}{V}\sqrt{\frac{xl\beta}{k_n V_{GT} f[C_g + (C_{ox} l + 2C_0)]}}. \tag{42}$$

According to expressions (41) and (42), the transistor gate widths depend on the sourcing current, therefore, also depend on the load circuit according to Figure 7. Thus, the optimum parameters of transistors change with their load circuit. Therefore, it is important to derive during process the load capacitor allowing a better efficiency (i.e., a maximal transfer of supply power to the load) and the corresponding average current which will permit an optimum geometric parameter evaluation. So in the following line, we will derive the design method yield to the better power transfer efficiency and the corresponding supply current for the optimum geometrical parameter calculation.

Let us suppose that in the CMOS integrated circuit, the various elementary circuit structures have loads capacitor of the same values C (gate capacitor in general) as shows in Figure 7, and a corresponding parasitic capacitor αC. The coefficient α represents in general the term which binds the current losses I_{leack_ch} and the total load capacitor C, it is generally higher than zero for real circuits. Therefore, the total supply current can be defined by (43),

$$i_D(t) = i_{ch}(t) + I_{leack\_ch}, \tag{43}$$

with

$$I_{leack\_ch} = \alpha CfV \tag{44}$$

and V is the control voltage of the load current i_{ch},

$$i_{ch}(t) = C\frac{dV(t)}{dt}. \tag{45}$$

From Figure 8, we can derive (46) below,

$$i_D(t) = \frac{V_{DD} - V(t)}{R_{on}}. \tag{46}$$

From (43), (44) and (46), we have derived (47) below which is the differential equation for control voltage V calculation,

$$\frac{V_{DD} - V(t)}{R_{on}} = C\frac{dV(t)}{dt} + \alpha CfV(t). \tag{47}$$

The resolution of (47) yields to the control voltage given by (48),

$$V(t) = \frac{V_{DD}}{1 + \alpha R_{on}Cf}\left[1 - \exp\left(-\frac{1 + \alpha R_{on}Cf}{R_{on}C}t\right)\right]. \tag{48}$$

The following charge current expression (49) is just deriving according to (45),

$$i_{ch}(t) = \frac{V_{DD}}{R_{on}} \exp\left(-\frac{1+\alpha R_{on}Cf}{R_{on}C} t\right). \tag{49}$$

Finally, the total supply current $i_D(t)$ is obtained by (50) according to (46),

$$i_D(t) = \frac{V_{DD}}{R_{on}}\left[1 - \frac{1}{1+\alpha R_{on}Cf}\left(1 - \exp\left(-\frac{1+\alpha R_{on}Cf}{R_{on}C} t\right)\right)\right]. \tag{50}$$

For a minimum loss in power transfer to the load, the efficiency (which is the ratio of the load power to the total supply power) given by (51) most tend to one,

$$Efficiency = \frac{P_{load}}{P_{supply}} = \frac{I_{ch}V}{I_D V_{DD}}. \tag{51}$$

From (48), (49) and (50), we obtain

$$Efficiency = \frac{R_{on}\, b/a\,[1-\exp(-a)][1-1/a[1-\exp(-a)]]}{1+b/a\,[1-a-\exp(-a)]} \tag{52}$$

with *a* and *b* the defining constant below; χ/f is the circuit element response time,

$$a = \chi \frac{1+\alpha R_{on}Cf}{R_{on}Cf} \quad \text{and} \quad b = \frac{1}{1+\alpha R_{on}Cf}.$$

According to (52), we will simply during the process, for a choosing constant α $(0 \le \alpha \le 1)$ and an expected response time χ/f, derived the conduction resistance Ron and corresponding load capacitor *C* whose lead to a better efficiency; the deduced average current in the following according to (50) will then be used in the optimum geometric parameter calculation. Therefore, for optimum energy consumption during the design process, the circuit designs most progressively move from the load element estimation. We have in Figure 10(a), the efficiency variation with the load circuit capacitor for various conductions resistance values, in Figure 10(b), a derived average supply current variation with the load capacitor for the same various conductions resistance values.

From this figure, for an example of circuit operating at a frequency of 10 MHz, for an expected response time element circuit of 0.1ns (i.e., $\chi = 0.001$) and $\text{Ron} = 0.9\,\text{Ohm}$, the load capacitor of 40 fF allows an efficiency of 60.8% for an expected average total supply current value of 0.6mA. According to Figure 8, this current estimation should be used to calculate the optimum geometric parameter of element circuit1 of which load must be an input impedance capacitor *C* of an element circuit2.

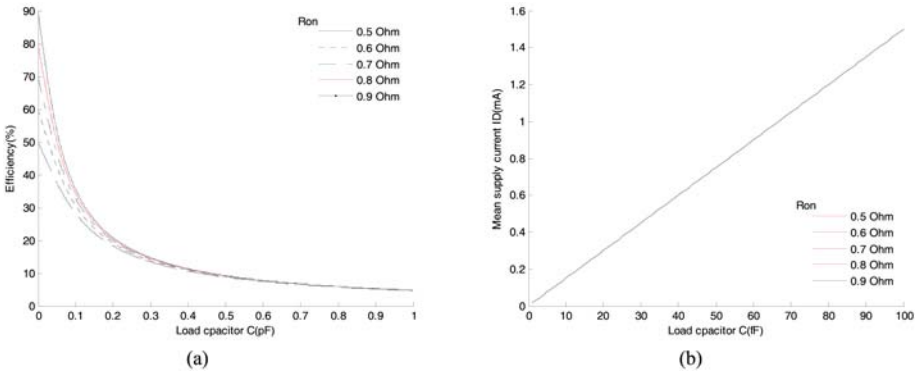

Figure 10. (a) Power transfer efficiency variation with the input load circuit impedance (capacitor C) for various conductions resistance values; (b) Load current mean value variation with the load capacitor for various conductions resistance values; $f = 10\text{MHz}$; $V_{DD} = 1.5V$; $\alpha = 0.2$; $\chi = 0.001$.

5. Future Work

One of the challenges in the electronic circuit design implementation is the appropriate energy consumption estimation. Essentially, the control circuitry power level expected will involve along with design process and no at the final circuit test as usually. In order to improve efficiency of handy PLL application using very low voltage battery (<1.5V), the power consumption control circuitry model in simulator must be designed. In general, the theory presented in this paper can be applied to any process which allows selection of PLL elements. So, future work would be towards implementation of simulation model of PLL consumption for power control circuitry during design.

6. Conclusion

We have presented in this paper the model types and expressive power consumption in a PLL system. The global PLL model is the synthesis of each typical circuits functional block model, its bases on models being and energy losses forms of the elementary components. Its interest is not any more to show, especially in medical electronics where the need of pacemaker design with the battery long lifespan is a major asset. This work can be adapted to any electronic system (with typical structure used) design process in order to carry out a preliminary energy expenditure estimation and optimization for a low final power consumption circuit.

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