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RECONFIGURABLE SIGMA DELTA A/D CONVERTER FOR SOFTWARE RADIO RECEIVER

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Abstract

Reconfigurable systems are attractive implementation platforms for many applications due to their capability of offering high performance, low development costs and short design times, while being accessible to less experienced designers. It is essential to develop efficient techniques for designing reconfigurable analog to digital converters (ADC) due to the importance of ADCs in software radio systems. Analog to digital converters are ubiquitous critical components of all signal processing systems. This paper presents the design and simulation results of a reconfigurable sigma delta ADC for software radio systems.

1. Introduction

A single wireless user terminal should be designed, which can automatically operate in different heterogeneous access networks. The 3G wireless receivers have to be compatible to 2G systems also. Therefore, the 3G wireless receivers have to be reconfigurable for multiple standards. The A/D converter in the receiver path is the bottleneck portion because of the significant channel bandwidth differences between 2G and 3G standards.

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Future mobile terminals become multimode communication systems. In order to handle different standards, this technique proposed to perform baseband processing in heterogeneous reconfigurable hardware. This multimode communication is not only the baseband processing but also error decoding and differs for every type of communication system. Effective quantization of the radio signal at the antenna enables fast reconfiguration of the air interface parameters of the communication terminals. This dynamic switching of frequencies and communication protocols in the user's terminals provide the remote reconfiguration of the terminal by adding or removing system software components with the result giving greater flexibility. Several DSP techniques are instrumental in obtaining high execution speeds. We take advantage of last technological progress in ADC design.

The ADC is an important element for digital signal processing system. The heart of an ADC is high resolution for precise representation of the original signal and high bandwidth for fast processing [5]. Conventional ADC architectures, e.g., flash; 2-step flash and successive approximation are not suitable for high-resolution applications because of the need of near ideal analog components and precise trimming [4]. To implement a high resolution A/D converter, the sigma delta modulator is considered a suitable approach (in Figure 1) and widely used due to its simplicity and effectiveness.

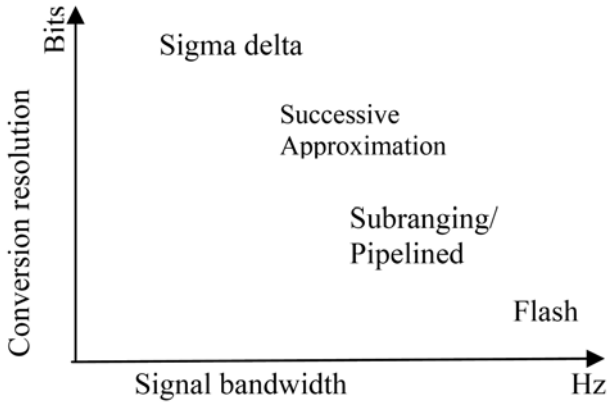


Figure 1. Bandwidth resolution tradeoffs.

An architecture that may be suitable for the digital front end of a multiband, multimode SDR (Software Defined Radio) is proposed. SDR provides an efficient and relatively inexpensive solution to the design of multimode, multiband, multi

functional wireless devices that can be enhanced using software upgrades only. The advantage of the SDR template is the possibility to implement real adaptive systems. Research in Software Defined Radio focuses strongly on multimode communication systems [7].

Building of a reconfigurable SDR system introduces new challenges in hardware and software designs. The primary goal of an SDR based system is to maximize flexibility. SDR based systems provide a large percentage of their functionality in software. This requires that the systems be built using general purpose hardware components that can easily be reprogrammed to assume new behaviour [6].

The paper is organized as follows: Section 1 is the introduction. Section 2 gives the reconfigurable receiver architecture of software radio. The performance of sigma delta modulator is discussed in Section 3. Section 4 provides the simulation results and finally Section 5 concludes the paper.

2. Reconfigurable Receiver Architecture

Software Defined Radio denotes wireless communication systems that are characterized by an analog front end followed by a programmable, digital baseband processing part. In the analog front end the radio signal is received, filtered and amplified. The filtered, amplified radio signal is converted to digital samples by sigma delta converter. The sigma delta converter is the proposed part in this paper. Multi-standard analog-to-digital converters for wireless receivers have recently gained a lot of research interests [1]. In particular, the sigma delta modulator is an attractive analog-to-digital converter architecture for such a wireless receiver. However, next generation reconfigurable TRF (Tuned Radio Frequency) transceivers should also adapt to the environment (signal strength, presence of blocker, battery power, etc.). The analog-to-digital converter therefore needs to be dynamically adaptive and not only needs to switch statically between different communication standards.

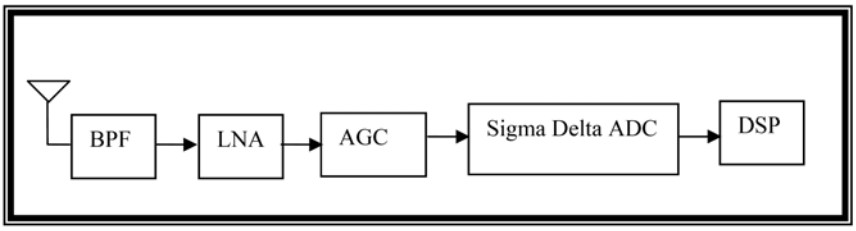


Figure 2. Tuned radio frequency receiver.

The TRF receiver is better suited for a software radio that supports multiple air interface modes [8] and multiple bands than the single conversion receiver and particularly than the heterodyne receiver because the filter requirements for the IF stages make it difficult to support the multiple bandwidths that might be required of a multimode receiver.

The Tuned Radio Frequency (TRF) receiver, shown in Figure 2, consists of an antenna connected to an RF bandpass filter (BPF). The BPF selects the signal and the LNA with the automatic gain control (AGC) raises the signal level for the compatibility with the ADC. The ADC must accommodate multiple signals over the wide bandwidth and high dynamic range. For this purpose, single-stage sigma delta A/D converters have been proposed to be an excellent solution as the required resolution of a specific standard may be achieved by adjusting the number of bits in its internal quantizer or the over sampling ratio.

3. Performance of Programmable ADC

Sigma delta conversion is a technique that has gained popularity for high resolution applications. The system consists of an analog sigma delta modulator followed by a digital decimator as shown in Figure 3:

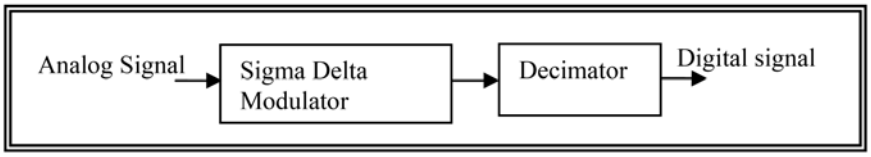


Figure 3. Block representation of sigma delta ADC.

The sigma delta modulator samples the analog input at many times the Nyquist rate and produces a 1-bit output whose average value tracks the analog input. This 1-bit data stream is processed by a digital filter to produce a high resolution conversion result. The modulator consists of an integrator, a quantizer and a DAC (unit gain) used in the feedback path as shown in Figure 4. The filter mostly used for the back end of a sigma delta converter is the FIR, because of its stability; ease of implementation, linear phase response and the fact that decimation can be incorporated into the filter itself. The process of decimation is used in a sigma delta converter to eliminate redundant data at the output.

The implementation of the sigma delta ADC has been chosen for three reasons: firstly, the continuous time ADC has lesser power consumption, then the ADC has

an inherent anti-aliasing filter and finally a programmable gain can be included in the ADC [2]. According to the different signal bandwidth and dynamic range requirements, the sigma delta modulator is reconfigured to achieve the required resolution with less power consumption. Sigma delta modulators naturally provide the trade off between speed (Over Sampling Ratio) and resolution [3].

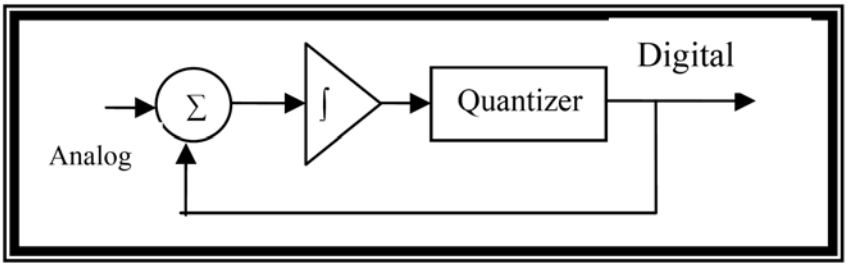


Figure 4. Sigma delta modulator.

Sigma delta modulators are very popular in wireless communication and multi-standard transceivers because of their ability to provide high resolution with relatively low precision components. Sigma delta modulators have either single loop or cascaded (MASH) structure. Cascaded sigma delta structures realize high-order noise shaping by cascading sigma delta stages of second order or first-order to avoid instability. The SNR response of first, second and cascaded sigma delta modulator signals are shown in Figure 5. The SNR responses are more or less same for both second order modulator and cascaded modulator. When increasing the order of modulator will lead a stability problem, in such a case, cascade modulator is the best way to implement in the receiver for wide bandwidth and also provide good resolution.

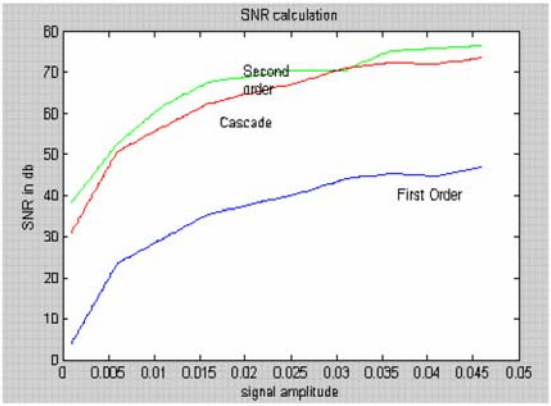


Figure 5. SNR response of sigma delta ADC.

Parameters of sigma delta ADC

The input signal bandwidth (–3dB) f_B is defined as the value between –*fs* to *fs* and OSR is defined as the ratio between *fs* to $2f_B$, where *fs* is the sampling frequency and f_B is the input signal bandwidth. Good resolutions are achieved with the increase of OSR. Increasing the sampling rate can be used to improve the SNR of the system as shown in Figure 6. By increasing the orders $(0, 1, ..., 5)$ better SNR value is achieved with less OSR value which indicates the minimum bandwidth. As the sampling rate is increased, the quantization noise power remains constant. The resolution of the converter indicates the number of discrete values it can produce over the range of analog values.

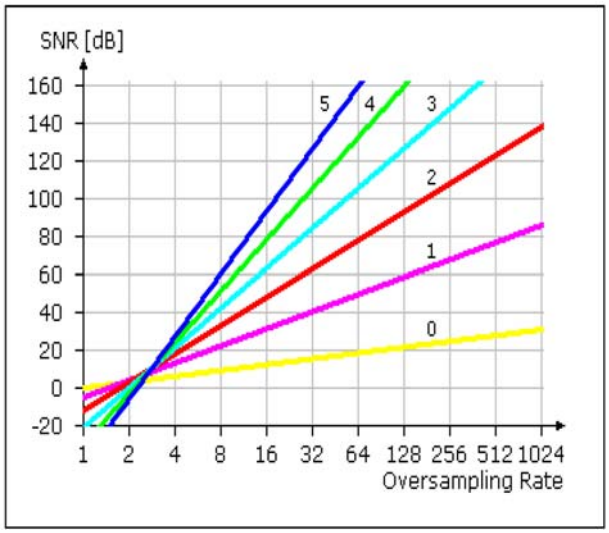


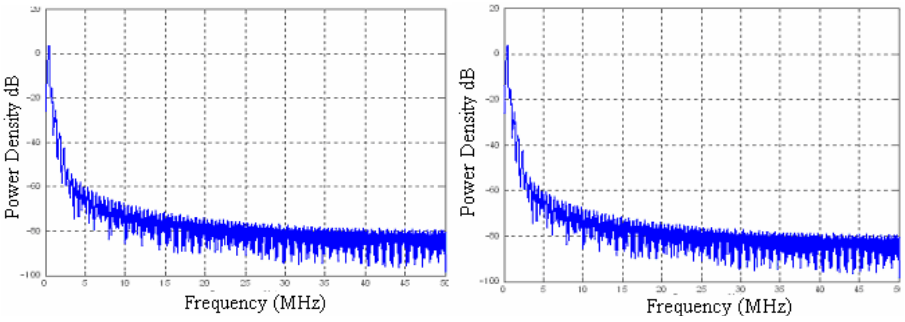
Figure 6. SNR vs. OSR of different orders.

The use of a second order modulator gives better noise shaping more noise is pushed outside the band of interest that leads to better resolution. A second order modulator gives a 15dB increase in resolution for every doubling of the sampling rate compared to 9dB for a single order system, this allows high resolutions to be achieved with lower sampling rates. The SNR with a full scale sine wave input will be (6.02N + 1.76)dB. If the ADC is less than perfect, and its noise is greater than its theoretical minimum quantization noise. For sinusoidal inputs, the dynamic range of the ADC is defined as the ratio of the signal power of a full scale sinusoid to the signal power of a small sinusoidal input that results in a SNR of 1 or 0.

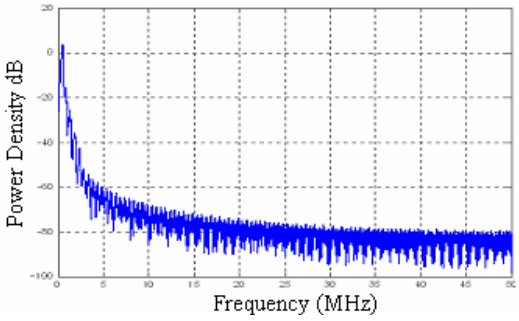
4. Experimental Results and Measurements

A sigma delta modulator is designed to meet the requirements of reconfigurable ADC in the TRF receiver structure. The proposed sigma delta modulator is implemented by using MATLAB 7.1 and Simulink Model. For different signal (100KHz to 800MHz) standards, sinusoidal input signals are applied to the modulator and the simulation is run to obtain enough data points.

This ADC has a wider dynamic range than the absolute minimum, which allows the system to shift part of the programmable gain and filtering requirements from the analog domain to the digital domain, where programmability is much easier. Figure 7 shows the frequency response of the three different modulator outputs. The frequency ranges of the *x*-axis are up to half of the input sampling frequency.



(a) First order (b) Second order



(c) Cascade section

Figure 7. Frequency responses of different sigma delta modulators.

Table 1 shows the performance of different orders in sigma delta ADC for software radio in TRF receiver. Simulations for the designed 4th order (2-2) modified cascaded sigma delta modulator were performed using 16 bit, the SNR achievable is 101.9 and the SNR for second order ADC is 98.8. To improve the SNR, increase the number of order with the same resolution, which also support for different standard signals. The cascaded modulator is suitable for software radio to provide Good SNR value and more flexibility for different standard signals.

Table 1. Sigma delta performance in SDR

Order	Resolution	SNR in dB
First	12	74.9
Second	16	98.8
Cascade (2-2)	16	101.9

5. Conclusion

Implementation considerations based on the sigma delta analog-to-digital converter (ADC) technologies are discussed, together with digital signal processing techniques. A sigma delta modulator is designed to meet the requirements of a reconfigurable receiver for different standard signals from 100KHz to 800MHz high resolution and low power consumption can be achieved by using a lower order multi-bit sigma delta modulator.

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