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ON THE LOW-COMPLEXITY ARCHITECTURE OF ROBUST CHANNEL ESTIMATION FOR A TIME-VARYING CHANNEL

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Abstract

This paper describes a robust channel estimation architecture for a WCDMA system. The robust channel estimation architecture consists of a phase variation measurement unit, a filter-parameters generator and an adjustable channel filter. The phase variation measurement unit estimates the Doppler shift of the fading channel. Using the estimated Doppler shift, the filter-parameters generator maps the corresponding filter parameters for the adjustable channel filter. Additionally, we propose a two-stage phase rotation architecture for calculating the carrier phase of the pilot signal. This two-stage phase rotation architecture has low complexity and can be implemented by adders/subtractors and shift registers. To evaluate the hardware complexity of the proposed architecture, an FPGA design is also proposed to implement the robust channel estimation architecture. The simulation results show that the bit error rate of the RAKE receiver with utilizing the proposed channel estimation architecture performs well in a time-varying channel.

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1. Introduction

Wideband Code Division Multiple Access (WCDMA) is a promising technology to provide a higher system capacity and a wide range of multi-media services worldwide [10]. In general, a WCDMA system utilizes a pilot signal to estimate the multi-path channel response by a channel estimation filter. The estimated channel response is provided to compensate the fading channel within the RAKE combine. Conventionally, there are several simple channel estimation filters, such as a moving average (MA) filter and a first-order infinite impulse response (IIR) filter. To prevent the occurrence of the error floor in the bit-error performance, the bandwidth of the channel estimation filter would be wide enough to accommodate the spectrum of the pilot signal in the fading channel. In contrast, the channel estimation filter would generate the output with the excess noise as if the bandwidth of the channel estimation filter is too wide. In [13], the Wiener filter is the optimal channel estimation filter for a given Doppler frequency. However, the Wiener filter cannot be optimal as the Doppler frequency of the fading channel is varied.

To combat the fading channel with a changed Doppler shift, some adaptively filtering methods which include the least mean square (LMS) algorithm and the recursive least square (RLS) algorithm were previously proposed in [7, 13]. But these adaptive methods are too complex to implement in practice. Various techniques to estimate the velocity of the mobile for a mobile communication channel were proposed to enhance the accuracy of the Doppler frequency estimation [1, 4, 8]. But these complicated signal processing methods are not adequate for the channel estimation. There are several previous literatures to estimate the Doppler shift and adjust the channel filter coefficients for a time-varying channel [2-3, 6, 9]. In [2, 6], the level crossing rate detector was utilized to estimate the fading rate but severely degraded the performance with the noise effect. Oh and Cioffi utilized a decimation method and a digital bandpass filter to estimate the vehicle speed of the mobile [9]. The decimation process is simple but the digital bandpass filter needs more complexity to extract the output energy of the decimated signal. Choi and Lee proposed a statistical method to estimate the maximum Doppler

frequency of the channel [3]. In [3], the authors first calculated the auto-correlation of the received pilot signal and set a threshold to decide the zone of the fading rate. The operation of the auto-correlation consumes high computation power for multiplications and is not practical in implementation. In this paper, we propose a robust channel estimation architecture with low complexity. Unlike the conventional architectures, the proposed architecture first calculates the averaged carrier phase difference of the pilot signal to estimate the Doppler frequency. We then divide several zones for the ranges of the Doppler frequency and map the appropriate channel filter parameters which can be pre-calculated and stored. In addition, we propose a two-stage phase rotation algorithm to perform the carrier phase calculation. The two-stage phase rotation algorithm is a CORDIC (Coordinate Rotation Digital Computer) [12] based design which just needs shift-and-add operations in hardware implementation.

The rest of this paper is organized as follows. Section 2 provides the system description. In Section 3, we proposed the robust channel estimation architecture. Computer simulations and the performance of the proposed robust channel estimation architecture are presented in Section 4. Finally, we give some conclusions in Section 5.

2. System Model

The system considered in this paper is based on a WCDMA downlink system. We assume the transmitted signal consists of a dedicated physical channel (DPCH) and a common pilot channel (CPICH). More specifically, the baseband transmitted signal $s(t)$ can be expressed by

$$s(t) = \sum_{i=0}^{\infty} \sum_{n=0}^{N_d-1} [d_i C_d(n) + \sqrt{G_p} C_p(n)] C_s(m) U(t - nT_c - iT_s),$$

$$m = (i \cdot N_d + n) \text{ module } (38400) \qquad (1)$$

where N_d is the spreading factor for the data channel, d_i is the i-th QPSK data symbol $(\pm 1/\sqrt{2} \pm j \cdot 1/\sqrt{2})$, G_p is the pilot channel power gain relative to the data channel, C_d and C_p are the Walsh codes for the

data channel and the common pilot channel respectively, C_s is the cell-specified scrambling code, T_c is the chip period, T_s is the data symbol period and $U(t)$ is a unit-amplitude rectangular pulse of duration T_c. The transmitted signal then passes through a multi-path fading channel which is modeled as L-tapped delay line with uncorrelated complex coefficients $h_l(t)$ and path delays $\tau_l T_c$, $l = 0, 1, \Lambda, L-1$. The uncorrelated complex coefficient $h_l(t)$ represents the fading gain of the multi-path fading channel for the l-th path. In general, the fading rate of the uncorrelated complex coefficient increases with the Doppler-shift due to the mobile speed. Additionally, the uncorrelated complex coefficients are assumed with magnitude subject to Rayleigh distribution and with phase subject to uniform distribution. All the path delays are assumed to be multiples of the chip time in our system. The received signal can be described by

$$\tilde{r}(t) = \sum_{l=0}^{L-1} h_l(t) S(t - \tau_l T_c) + w(t), \tag{2}$$

where $w(t)$ is the zero-mean complex Gaussian noise with two-side power spectral density $N_0/2$. To simplify the receiver design, we assume the received signal $\tilde{r}(t)$ is sampled by the chip rate. The sampled signal $r(n)$ can be represented by

$$r(n) = \sum_{l=0}^{L-1} h_l(n) S(n - \tau_l) + w(n), \tag{3}$$

where n is the chip time index.

3. Robust Channel Estimation Architecture

The proposed robust channel estimation architecture shown in Figure 1 contains a phase variation measurement unit, a filter-parameters generator and an adjustable channel filter. The phase variation measurement unit is employed to estimate the Doppler shift of the carrier frequency in the time-varying channel. The filter-parameters generator is to map the estimated Doppler shift into the parameters for the adjustable

channel filter. The despread pilot signal $y_p(k)$ then passes through the adjustable channel filter with the input filter-parameters. The output of the adjustable channel filter is the estimated channel response. In the next, we will describe the block diagram of the proposed channel estimation architecture in detail.

3.1. Phase variation measurement unit

Figure 2 shows the block diagrams of the phase variation measurement unit. The despread pilot signal $y_l(k)$ for the l-th path at the k-th symbol period firstly passes through a first-order IIR filter to suppress the noise level. The real part and the imaginary part for the IIR filter output can be obtained by

$$\hat{y}_{l,I}(k) = \alpha_f \hat{y}_{l,I}(k-1) + (1-\alpha_f) \cdot y_{l,I}(k), \tag{4}$$

$$\hat{y}_{l,Q}(k) = \alpha_f \hat{y}_{l,Q}(k-1) + (1-\alpha_f) \cdot y_{l,Q}(k), \tag{5}$$

where α_f is the filter parameter, $y_{l,I}(k)$ and $y_{l,Q}(k)$ are the in-phase component and the quadrature phase component of $y_l(k)$, respectively. After the phase calculator computing the carrier phase of the filtered signal $\hat{y}_l(k)$, we get the phase difference magnitude by

$$\Delta\phi_l(k) = |\, \phi_l(k) - \phi_l(k-1) \,|, \tag{6}$$

where $\phi_l(k)$ is the estimated carrier phase for the l-th path signal at the k-th symbol time period. The estimated Doppler shift in a time-varying channel can be obtained by averaging the magnitude of the phase difference for a MT_s time period, where M is a system parameter. For the i-th MT_s time period, the phase variation measurement unit generates an estimated Doppler shift by

$$f_i = \frac{1}{2\pi ML} \sum_{l=0}^{L-1} \sum_{m=0}^{M-1} \Delta\phi_l((i-1) * M + m). \tag{7}$$

To reduce the hardware complexity, we propose a two-stage phase rotation architecture to implement the phase calculation within the phase variation measurement unit. The two-stage phase rotation architecture is

based on an iterative methodology of performing vector rotations. Without loss of generality, we would map the input complex signal $\hat{y}_l(k)$ to the vector in a Cartesian plane by (x, y) in the following as we describe the operations of the two-stage phase rotation, where $x = \hat{y}_{l,I}(k)$ and $y = \hat{y}_{l,Q}(k)$.

3.2. Two-stage phase rotation architecture

Figure 3 shows the block diagram of the two-stage phase rotation architecture. Prior to performing the phase rotation, we transform the input vector signal (x, y) to the vector (x', y') such that the angle of the transformed vector (x', y') is restricted between 0 to $\pi/4$. Table 1 depicts the mapping of this vector transformation. With the input vector (x, y), we can obtain the transformed vector (x', y') and the state value q by looking up the table. The transformed vector (x', y') is provided for the succeeded stage I phase rotation. The state value q denotes the octal phase of the input vector (x, y) and is provided for the phase de-mapping process. This initial vector transformation induces no phase error and makes the phase rotations more effective for the input vector signal in the Cartesian plane.

In stage I phase rotation, the input vector (x', y') performs the rotations by the elementary angle of ϕ_1 in the direction of clockwise. To reduce the computational power of the rotations, we set the elementary angle ϕ_1 to be $\tan^{-1}(2^{-n_1})$, where n_1 is a positive integer for the system parameter. The mathematical representation of the vector signal by rotating the phase ϕ_1 can be described by

$$x'_1 = \cos\phi_1(x' + 2^{-n_1} \cdot y'), \tag{8}$$

$$y'_1 = \cos\phi_1(y' - 2^{-n_1} \cdot x'). \tag{9}$$

From equations (8)-(9), we can find that the rotated vector (x'_1, y'_1) has a scalar factor of $\cos(\phi_1)$ with its magnitude. If we emphasize on the phase information of the rotated vector signal, we can derive the

mathematical representation of the iterative rotation by

$$x'_{n+1} = x'_n + 2^{-n_1} \cdot y'_n, \tag{10}$$

$$y'_{n+1} = y'_n - 2^{-n_1} \cdot x'_n, \tag{11}$$

where (x'_n, y'_n) denotes the rotated vector after the n-th rotation and the initial vector (x'_0, y'_0) is set to the input vector (x', y'). From equations (10)-(11), the iterative phase rotation is reduced to simple shift-and-add operations. In this stage, we would stop the iterative phase rotations by the elementary angle ϕ_1 as the magnitude of the y-component for the rotated vector is less than $2^{-(n_1+1)}$. The angle of performing all the phase rotations can be obtained by

$$\theta_1 = m_1 \cdot \tan^{-1}(2^{-n_1}), \tag{12}$$

where m_1 is the number of the iterative rotations in this stage. The elementary angle $\tan^{-1}(2^{-n_1})$ can be pre-calculated and stored in the table to save the computational power. At the output of this stage, we can generate the rotated vector signal (x'', y'') and the angle θ_1, where $x'' = x'_{m_1}$ and $y'' = y'_{m_1}$.

To improve the accuracy of the estimated phase of the vector signal (x, y), we get further to perform the phase rotations by the smaller angle ϕ_2 in stage II phase rotation. In the same way, the angle ϕ_2 is set to be $\tan^{-1}(2^{-n_2})$ to save the computational power, where n_2 is a positive integer for the system parameter. In general, n_2 is set to be larger than n_1. The input vector (x'', y'') performs the phase rotations in the clockwise direction as the y-component of the input vector is positive. Conversely, the input vector (x'', y'') performs the phase rotations in the counterclockwise direction as the y-component of the input vector is negative. We can derive the iterative phase rotation by

$$x''_{n+1} = x''_n \pm 2^{-n_2} \cdot y''_n$$

(“+”: clockwise direction, “-“: counterclockwise direction), (13)

$$y''_{n+1} = y''_n \mp 2^{-n_2} \cdot x''_n$$

("-": clockwise direction, "+": counterclockwise direction), (14)

where the initial vector (x''_0, y''_0) is set to the input vector (x'', y''). The iterative operation would be stopped while the magnitude of the y-component for the rotated vector is less than $2^{-(n_2+1)}$. The output angle for performing all the rotations by the elementary angle of $\tan^{-1}(2^{-n_2})$ can be obtained by

$$\theta_2 = \pm m_2 \cdot \tan^{-1}(2^{-n_2}), \tag{15}$$

where m_2 is the number of the iterative rotations in stage II phase rotations, the positive sign is denoted by the rotations in the clockwise direction and the minus sign is denoted by the rotations in the counterclockwise direction. According to the output angles for both the stage I phase rotation and the stage II phase rotation, we can obtain the output of the rotated angle θ_3 by the summation of θ_1 and θ_2. The rotated angle θ_3 is then sent through the phase de-mapping process to modify the rotated angle θ_3 by the state value q of the input vector (x, y). We can obtain the output of the phase calculation θ_{out} for the input vector signal (x, y) by Table 2. This output phase is applied for the output of the phase calculation within the phase variation measurement unit. For this two-stage phase rotation operations, the system parameters n_1 and n_2 would be related to both the power consumption and the phase accuracy. Table 3 describes the maximum number of times the phase rotations are performed and the output phase error for the various elementary angles within the two-stage phase rotation algorithm. Considering both the computational power saving and the phase error reduction, we have an appropriate choice of $n_1 = 2$ and $n_2 = 5$ in our system.

3.3. Adjustable channel filters and filter-parameters generator

In our system, the conventional moving average (MA) filter and the first-order infinite impulse response (IIR) filter are two optional filters to implement the adjustable channel filter. With the MA filter, the output of

the channel filter can be represented by

$$y_o(k) = \frac{1}{2N+1} \sum_{n=-N}^{N} y_p(k-n), \tag{16}$$

where $(2N+1)$ is the number of taps for the MA filter and $y_p(k-n)$ is the despread pilot signal at the $(k-n)$-th symbol period. Since the MA filter has an estimation delay of NTs, we would buffer the despread data signal for the NTs time period in the data flow. To track the channel response accurately, the filter parameter N of the MA filter is decreased as the channel fading rate is increased. With the first-order IIR filter, on the other hand, the output of the channel filter at the k-th symbol period can be described by

$$y_o(k) = \alpha \cdot y_o(k-1) + (1-\alpha) \cdot y_p(k), \tag{17}$$

where α is the filter parameter and $0 < \alpha < 1$. The group delay of the first-order IIR filter is approximately $(1-\alpha)^{-1}$ [5]. In general, the filter parameter α should be decreased to track the channel response more closely as the fading rate of the channel is increased. Conversely, the filter parameter α can be increased to suppress the noise effectively in a slow-fading channel.

In the filter-parameters generator, the filter parameters of the channel filter would be automatically adjusted by the input estimated phase variation of the channel. To reduce the computation power in the filter-parameters generator, the filter parameters of the MA filter and the first-order IIR filter for various channel conditions can be pre-calculated and stored in a look-up table. In our system, the filter-parameters generator shown in Figure 4 divides m regions for the phase variation of the fading channel. For each region of the phase variation, we can map the corresponding filter parameters. Table 4 depicts the relationship between the phase variation of the fading channel and the corresponding filter-parameters. In Table 4, the forgetting factor α of the IIR filter can be set by the combination of the powers of 2 for simplifying the hardware design of the IIR filter. The output filter parameters are sent to the delay circuit and the adjustable channel filter.

3.4. FPGA implementation for the proposed architecture

To evaluate the hardware complexity of the proposed architecture, we utilize the Xilinx FPGA to implement the proposed channel estimation architecture. Figure 5 describes the word-lengths of the functional blocks in our hardware design. For the adjustable IIR channel filter, the filter parameter $(1 - \alpha)$ is set by

$$1 - \alpha = \sum_{i=1}^{6} c_i \cdot 2^{-i}, \tag{18}$$

where $c_i = 0$ or 1. Therefore, we can implement the adjustable IIR filter without any multipliers. Figure 6 shows the hardware architecture of the adjustable IIR filter. For the delay circuit, we control the symbol timing offset between the despread data signal and the channel estimation output. If we assume that the maximum timing offset is eleven symbol periods, the delay circuit shown in Figure 7 can be implemented by a multiplexer, a de-multiplexer, shift registers and a counter. The architecture of the phase variation measurement mainly contains the phase calculation circuit and the differential circuit. Figure 8 shows the architecture of the phase calculation circuit for the hardware design with utilizing the proposed two-stage phase rotation algorithm, the phase calculation circuit needs no multiplier to implement. A ROM table and some comparators can be used to implement the filter-parameters generator.

From the above descriptions of the functional blocks, we can find that the robust channel estimation architecture can reduce the hardware complexity with no use of multipliers. We implement the proposed channel estimation architecture by the Xilinx Virtex-II XC2V2000-FF896 for our hardware design. Table 5 describes the design summary of the robust channel estimation architecture for the two-path fading channel. In this design, we need two sets of the circuits mentioned above to process the channel estimation of the multi-path signals.

4. Computer Simulations and Discussions

In our simulations, a WCDMA system with a carrier frequency of 2.0GHz and a chip rate of 3.84Mcps was adopted as the modulation scheme. We assume the transmitted signal consists of a data channel and a common pilot channel. The pilot signal power gain G_p relative to the data signal power was set to 7dB. The spreading factors for both the data channel and the pilot channel were set to 256. A two-path Rayleigh fading channel was assumed in the channel mode. Each path was independently generated by Jakes' model [11] and was assumed to have the same average signal-to-noise ratio. In the phase variation measurement unit, the filter parameter α_f of the pre-filter was set to 0.875. In the two-stage phase rotation architecture, we set the elementary rotation angles of the stage I phase rotation and the stage II phase rotation to be $\tan^{-1}(2^{-2})$ and $\tan^{-1}(2^{-5})$ respectively. The averaged period MT_s of the phase difference was set to $(2048 \cdot T_s)$.

To investigate the proposed channel estimation architecture, computer simulations were carried out under different channel conditions. With the floating-point simulations, the adjustable MA filter and the adjustable first-order IIR filter were utilized to evaluate proposed channel estimation architecture individually. With the fixed-point simulations, the first-order IIR filter for the adjustable channel filter was used to evaluate the hardware design shown in Figure 5. We investigated the mean square error (MSE) performances of the channel estimation. Additionally, the bit error rate (BER) performances with applying the proposed channel estimation architecture in a WCDMA receiver were also investigated. For the BER evaluation, we adopted the maximum ratio combining (MRC) RAKE for data detection. Figure 9 shows the floating-point MSE performances. We can find that the MSE is less than –20dB as the Eb/N_0 is larger than 9dB. The MSE is decreased as the fading rate is decreased. In comparison with the adjustable first-order IIR filter, we can observe that the MSE performance for the adjustable MA filter is slightly better than the MSE performance for the adjustable first-order IIR filter

in a fast fading channel. Figure 10 shows the floating-point BER performance with the adjustable MA filter. The BER performance of the proposed channel estimation architecture nearly approaches the BER performance for the ideal channel estimation. The BER performance for the higher vehicle speed is slightly worse than the BER performance for the lower vehicle speed. Figure 11 shows the floating-point BER performances with an adjustable first-order IIR filter. The BER performance with an adjustable first-order IIR filter is slightly worse than the BER performance with an adjustable MA filter. However, the adjustable first-order IIR filter has a lower complexity in comparison with the adjustable MA filter. Figure 12 and Figure 13 show the fixed-point MSE performance and the fixed-point BER performance, respectively. We can observe that the fixed-point performances are very close to the floating-point performances.

5. Conclusions

In this paper, we propose a robust channel estimation architecture which can adjust the channel filter parameters according to the estimated carrier phase difference for a fading channel. In addition, a two-stage phase rotation architecture is proposed to compute the carrier phase of the received pilot signal. This two-stage phase rotation architecture can dramatically reduce the hardware complexity for estimating the Doppler shift of the time-varying channel. An FPGA implementation is also proposed for the hardware design of the robust channel estimation architecture. The proposed channel estimation architecture can be applied not only to WCDMA systems, but also to the general pilot-aided communication systems. The proposed channel estimation architecture was evaluated by computer simulations. According to the simulation results, the MSE of the estimation result is lower than –20dB. The BER performance of the RAKE receiver with utilizing our channel estimation architecture performs well under different fading channels.

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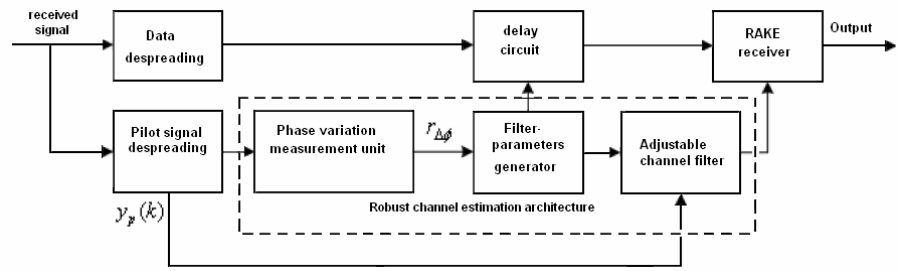

Figure 1. The robust channel estimation architecture for a WCDMA receiver.

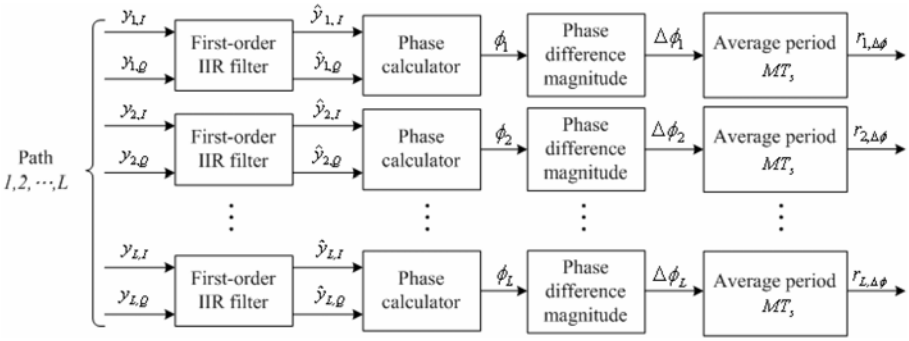

Figure 2. The phase variation measurement unit.

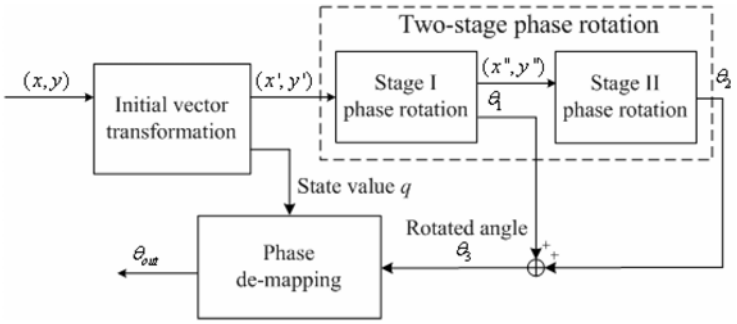

Figure 3. The two-stage phase rotation architecture.

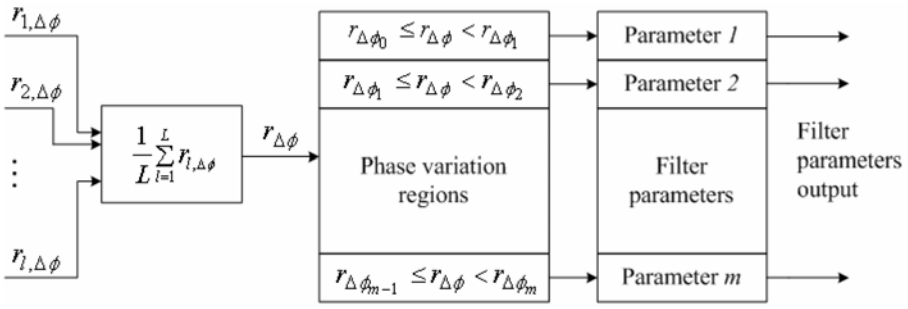

Figure 4. The filter-parameters generator.

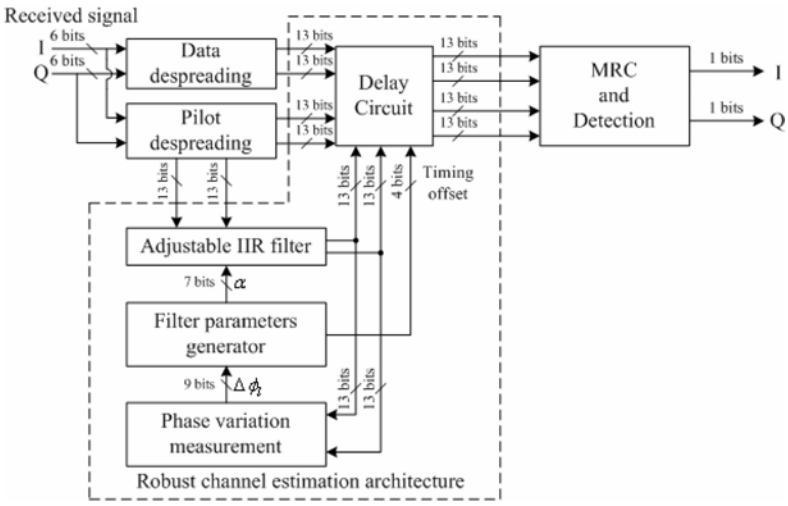

Figure 5. The functional blocks in our hardware design.

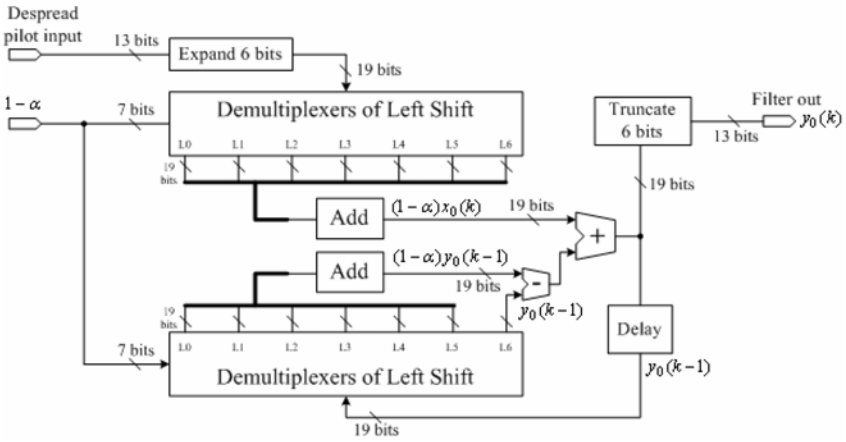

Figure 6. The hardware architecture of the adjustable IIR filter.

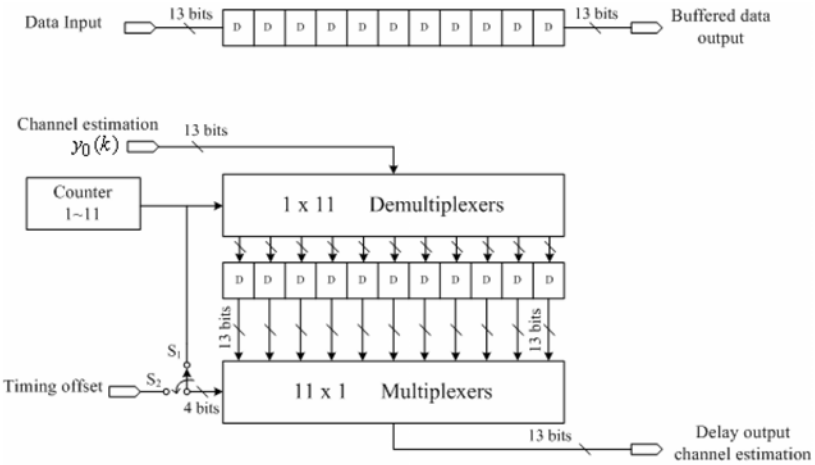

Figure 7. The delay circuit.

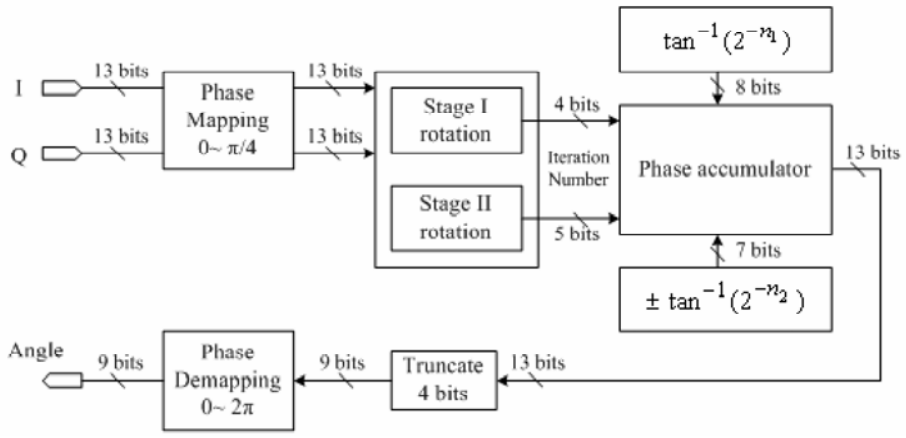

Figure 8. The hardware architecture of the phase calculation.

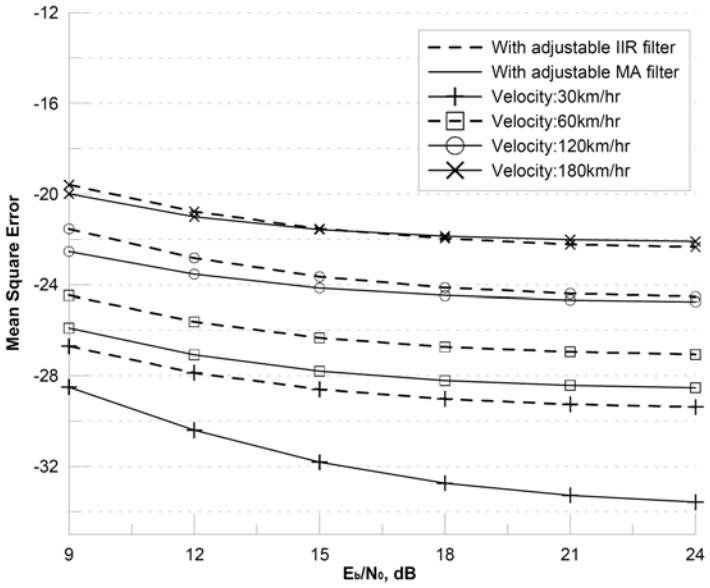

Figure 9. The floating-point MSE performances.

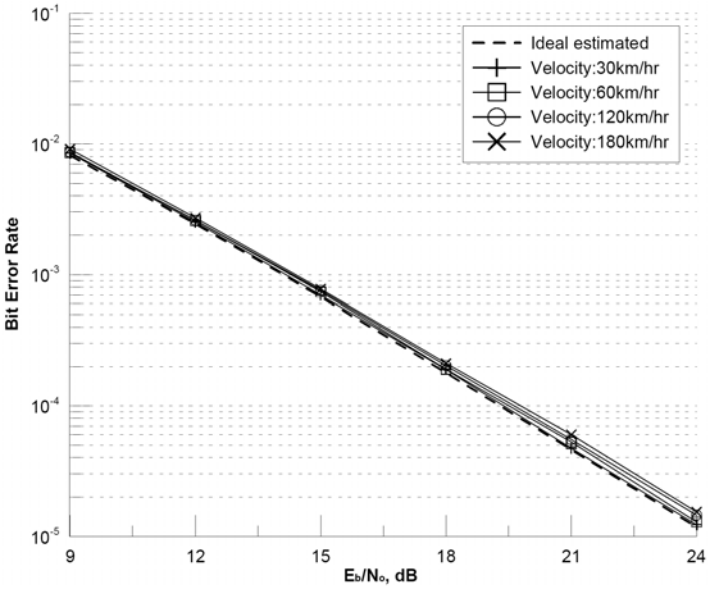

Figure 10. The floating-point BER performances with the adjustable MA filter.

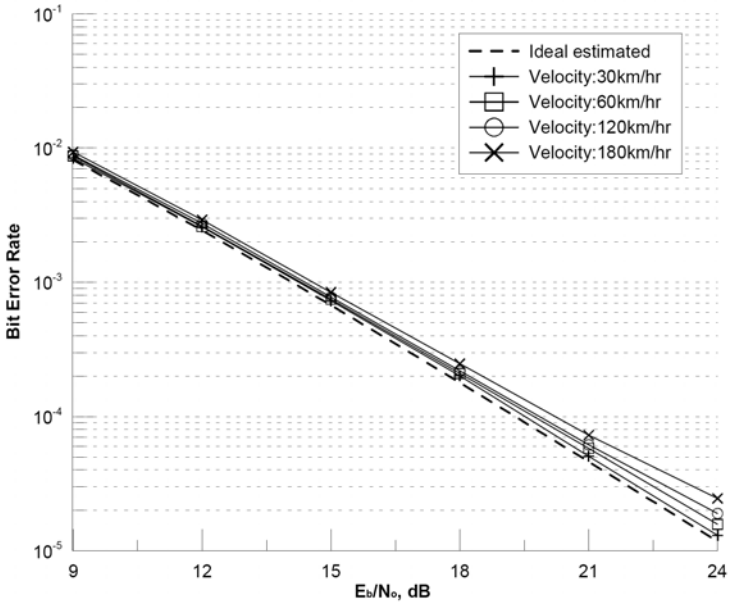

Figure 11. The floating-point BER performances with the adjustable first-order IIR filter.

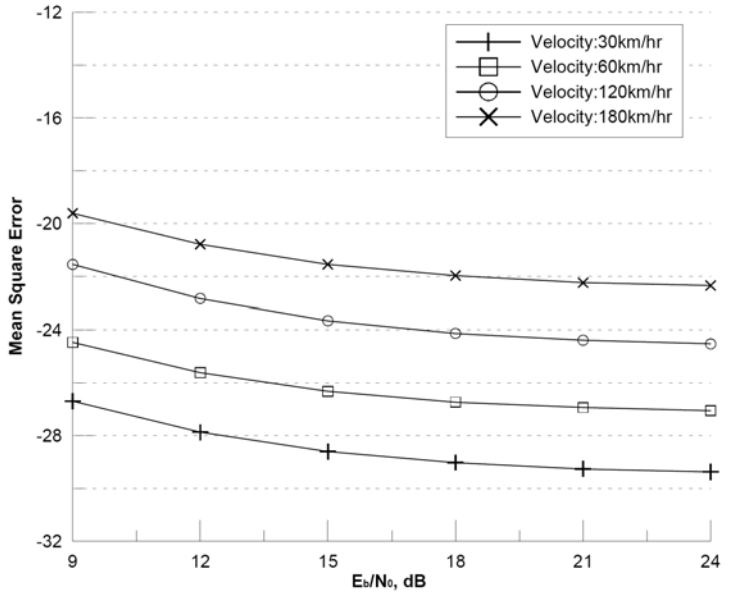

Figure 12. The fixed-point MSE performances with the adjustable first-order IIR filter.

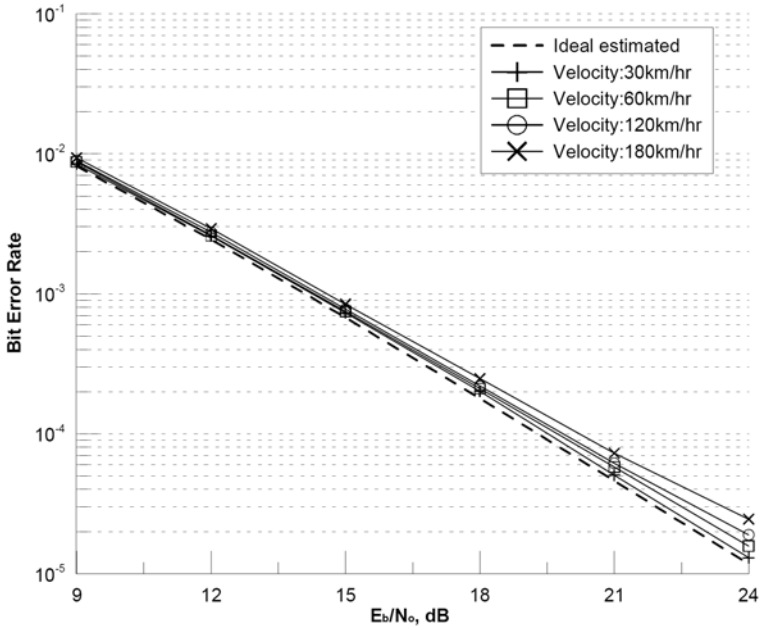

Figure 13. The fixed-point BER performances with the adjustable first-order IIR filter.

Table 1. The mapping of vector transformation

Sign of x	Sign of y	$\lvert \pi \rvert \leq \lvert y \rvert$	State value q	Transformed vector (x', y')	
+	+	False	0 0 0	$x' = x$	$y' = y$
–	+		0 1 0	$x' = -x$	$y' = y$
–	–		0 1 1	$x' = -x$	$y' = -y$
+	–		0 0 1	$x' = x$	$y' = -y$
+	+	True	1 0 0	$x' = y$	$y' = x$
–	+		1 1 0	$x' = y$	$y' = -x$
–	–		1 1 1	$x' = -y$	$y' = -x$
+	–		1 0 1	$x' = -y$	$y' = x$

Table 2. The demapping process for the output phase

State value q	Demapping process for θ_{out}
0 0 0	θ_3
0 1 0	$\theta_3 + \pi/2$
0 1 1	$\theta_3 + \pi$
0 0 1	$\theta_3 + 3\pi/2$
1 0 0	$\pi/2 - \theta_3$
1 1 0	$\pi - \theta_3$
1 1 1	$3\pi/2 - \theta_3$
1 0 1	$2\pi - \theta_3$

Table 3. The maximum number of iterative rotations and the output phase error

n_1 $\phi_1 = \tan^{-1}(2^{-n_1})$	n_2 $\phi_2 = \tan^{-1}(2^{-n_2})$	Maximum number of phase rotations for ϕ_1	Maximum number of phase rotations for ϕ_2	Output phase error (rads)
1	2	2	1	0.0125
	3		2	0.0625
	4		4	0.03125
	5		8	0.015625
2	3	3	1	0.0625
	4		2	0.03125
	5		4	0.015625
3	4	6	1	0.03125
	5		2	0.015625
4	5	13	1	0.015625
5		25		0.015625

Table 4. The relationship between the phase variation and the corresponding filter-parameters

Filter type	MA filter		IIR filter	
Parameters / $r_{\Delta\phi}$(rad / sec)	Average length (tap)	Symbol timing offset	Forgetting factor α	Symbol timing offset
0~0.50 (0~30 km/hr)	25	12	$1-(2^{-4}+2^{-6})$	11
0.05~0.08 (30~60 km/hr)	21	10	$1-2^{-3}$	7
0.08 ~ 0.115 (60~90 km/hr)	17	8	$1-(2^{-3}+2^{-4}+2^{-6})$	4
0.115~0.145 (90~120 km/hr)	11	5	$1-2^{-2}$	3
0.145~0.175 (120~150 km/hr)	9	4	$1-(2^{-2}+2^{-4})$	2
0.175~0.210 (150~180 km/hr)	7	3	$1-(2^{-2}+2^{-4}+2^{-5})$	2
>0.210 (>180 km/hr)	5	2	$1-(2^{-2}+2^{-3})$	2

Table 5. Robust channel estimation architecture design summary

Robust Channel Estimation Architecture Design Summary	
Logic Utilization:	
Number of Slice Flip Flops:	1,769 out of 21,504 8%
Number of 4 input LUTs:	8,305 out of 21,504 38%
Logic Distribution:	
Number of occupied Slices:	4,998 out of 10,752 46%
Number of Slices containing only related logic:	4,998 out of 4,998 100%
Number of Slices containing unrelated logic:	0 out of 4,998 0%
Total Number 4 input LUTs:	9,185 out of 21,504 42%
Number used as logic:	8,305
Number used as a route-thru:	880
Number of bonded IOBs:	66 out of 624 10%
IOB Flip Flops:	64
Number of Block RAMs:	5 out of 56 8%
Number of GCLKs:	1 out of 16 6%
Total equivalent gate count for design:	412,110
Additional JTAG gate count for IOBs:	3,168
Peak Memory Usage:	169MB
Minimum period:	146.533ns
Maximum Frequency:	6.824MHz

■