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A HIGH GAIN 2.45GHz VERY LOW NOISE AMPLIFIER WITH AN OPTIMIZED INPUT/OUTPUT IMPEDANCE MATCHING

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Abstract

A new design technique for high gain and low noise for 2.45GHz low noise amplifier is reported in this study. It consists of the use of diode connected PMOS transistor in the input instead of a resistor to obtain a good impedance matching with low noise figure and small area. This technique is studied theoretically and through simulation to be validated. The LNA operates at 1.8V. Its bandwidth is between 2.05 and 2.7GHz. It achieves at 2.45GHz frequency high voltage gain about 24.634dB with 0.98dB noise figure.

1. Introduction

In a receiver front-end, the low noise amplifier (LNA) is a critical block since it should amplify the weak signal received from the antenna with

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sufficient gain and little additional noise [1]. The low noise amplifier (LNA) has very stringent requirements such as a high linearity and a well-matched input impedance to be able to interface with the preselected filter that precedes the LNA [2]. To ensure an optimal matching of the source antenna power, the input impedance of the LNA has to be very close to purely resistive with a value near to 50Ω. However, because the LNA input is connected to a capacitive node, providing a good impedance match with the source without degrading the noise constraint is very hard to achieve [3, 4].

In recent years, several conventional structures have been used for real input impedance. Because of the resonance of inductor with the amplifier input capacitance at the desired RF frequency, in the parallel resistance input matching LNA, this resistance remains as the input impedance. In spite of its simplicity and due to a noise figure exceeding 3dB, this structure is used only in narrowband applications that do not have strict noise requirements [5]. The inductively degenerated common-source LNA uses inductive source or emitter degeneration to generate a real term in the input impedance. Tuning of the amplifier input becomes a necessity [6]. It is worth noting that the inductive source degeneration is the most prevalent method used for both narrowband and wideband LNAs [7]. The resistive feedback LNA provides a wideband input and output matching and a small die area because no inductor is required for the input matching. However, it has a poor NF and consumes a large amount of power [8].

Finally, the design used in this research study is the resistive termination architecture. Unfortunately, the use of real resistors in this way has a deleterious effect on the amplifier's noise figure [4].

The technique applied to overcome this problem is the use of diode connected transistor instead of a resistor. The effectiveness of this technique was demonstrated theoretically and by simulations for an LNA operated at 2.45GHz.

The remainder of this paper is organized as follows. In Section 2, we present an overview of designed LNA and forward a theoretical study of our technique. In Section 3, we validate it through simulation. Finally, Section 4 is devoted to draw some conclusions.

2. Circuit Description

2.1. LNA architecture overview

The architecture of the proposed LNA consists of matching the LNA at the input in a first step, then at the output in a second step to guarantee a desired signal along the circuit and at the output. The LNA transistor level implementation is presented by Figure 1. It shows that the input matching circuit contains only one inductance and two PMOS transistors. Both amplification stages have almost the same architecture, a driver NMOS transistor with its load impedance in the form of PMOS transistor. Both of the resistors and capacitors contribute to getting a good impedance matching and the desired bandwidth.

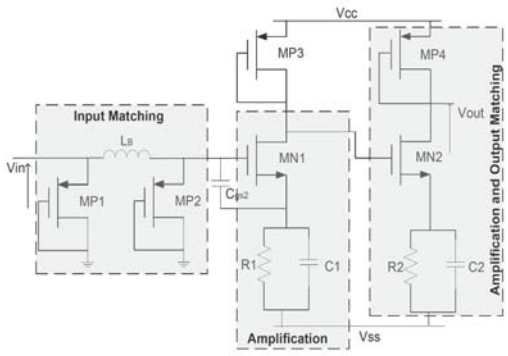

Figure 1. LNA transistor level implementation.

2.2. Input match circuit

To get a good input matching, the resistive termination LNA topology is used as presented in Figure 2(a):

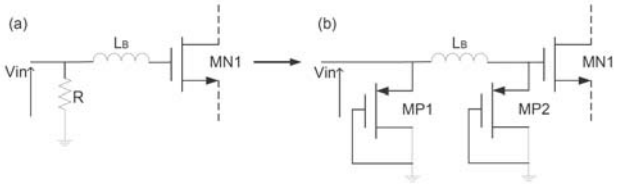

Figure 2. (a) Resistive termination LNA and (b) modified resistive termination LNA.

However, such architecture generates a lot of noise, to remedy this problem, the resistor was replaced by two diode connected PMOS transistors on both the sides of the inductor (Figure 2(b)). These transistors are operating in the saturation zone because the drain and the gate have the same potential.

We use the small signals diode connected PMOS transistor as shown in Figure 3(b) to get the PMOS impedance. To calculate the transistor impedance, the equation can be given as

$$R_{MP} = \frac{1}{\beta\left(\frac{W}{L}\right)(V_{gs} - V_{th})}, \tag{1}$$

where β is the transistor constant, W/L is the size ratio of $MP_{1\text{-}2}$, V_{gs} is the gate source voltage and V_{th} is the transistor threshold voltage. The small signals input matching circuit of LNA is presented in Figure 4.

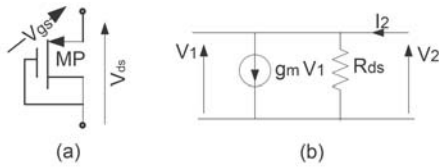

Figure 3. (a) Diode connected PMOS transistor and (b) small signal equivalent circuit.

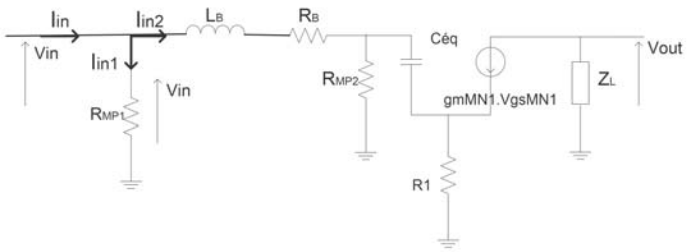

Figure 4. Small signals input matching circuit.

At the resonance frequency, the input impedance becomes equal to its real part as shown in (2):

$$Re(Zin) = \frac{1}{R_{MP1}} + \frac{R_{MP2} + R_B - \omega^2 L_B C_{eq}(1 + R_1)}{x} + A, \quad (2)$$

where A and x are given by (3) and (4), respectively,

$$A = \frac{\lfloor(\omega L_B + \omega R_{MP2} C_{eq} R_1) + (\omega C_{eq}(R_{MP2} + R_1))\rfloor}{x}, \quad (3)$$

$$x = [R_{MP2} - (\omega^2 L_B C_{eq}(1 + R_1))]^2 + (\omega L_B + \omega R_{MP2} C_{eq} R_1)^2. \quad (4)$$

C_{eq} is the equivalent capacitance of the association in parallel of C_{gs2} and C_{gsMN1} expressed by

$$C_{eq} = C_{gs2} + C_{gsMN1}. \quad (5)$$

Equation (2) shows that the input match quality can be tuned when R_{MP1}, R_{MP2}, L_B, C_{eq}, R_1 or R_B are varied. It also indicates that the variables R_{MP1} and R_{MP2} have great influence on the input impedance and, in particular, on values around the frequency 2.45GHz as shown in Figure 5 and Figure 6. The variation of these parameters was achieved by the variation of the widths (w) of transistors $MP1$ (W_{MP1}) and $MP2$ (W_{MP2}).

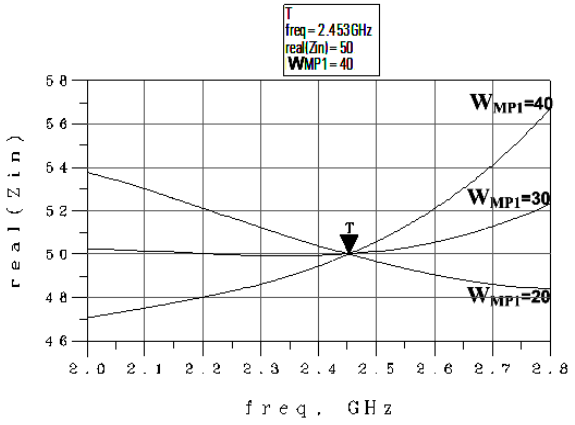

Figure 5. Influence of $W_{MP1}(\mu m)$ on the input impedance.

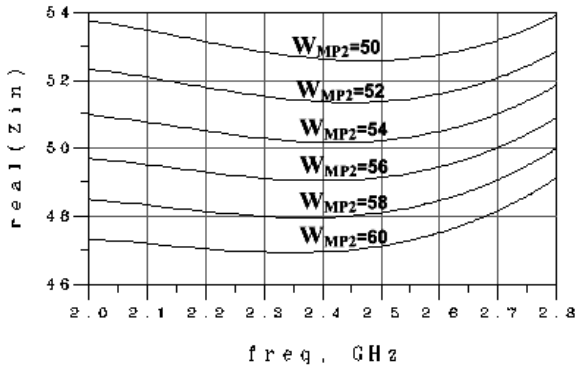

Figure 6. Influence of $W_{MP2}(\mu m)$ on the input impedance.

The previous figures demonstrate that the input impedance greatly depends on R_{MP1} and R_{MP2}. Thus, the use of this technique provides a very good and fine input adaptation.

2.3. Output match circuit

This block plays a dual role; amplification and output impedance matching. The small signals output matching circuit is presented in Figure 7.

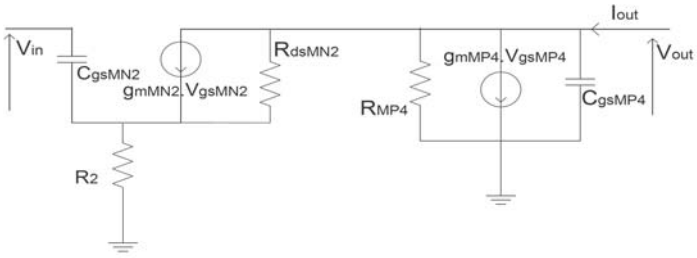

Figure 7. Small signals output matching circuit.

At the resonance frequency, the output impedance becomes equal to its real part as shown in (6):

$$Re(Zout) = (g_{mMN1} + v)\frac{1}{v^2 + z^2}, \tag{6}$$

where v and z are given by (7) and (8), respectively,

$$v = \frac{1}{R_{MP4}} + \frac{1}{R_{dsMN2}} + \frac{(\omega C_{gsMN2} R_2)^2 g_{mMN2}}{1 + (\omega C_{gsMN2} R_2)^2}, \tag{7}$$

$$z = \frac{C_{gsMN2} R_2 g_{mMN2}}{1 + (\omega C_{gsMN2} R_2)^2}. \tag{8}$$

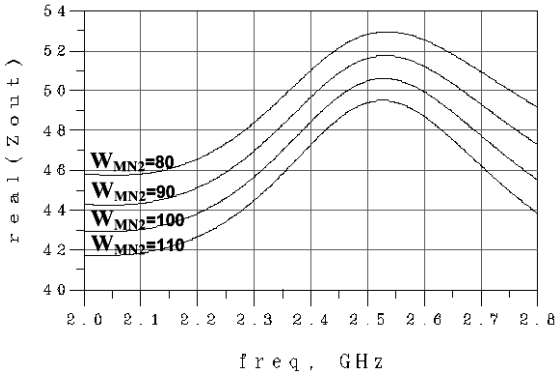

Figure 8. Influence of $W_{MN2}(\mu m)$ on the output impedance.

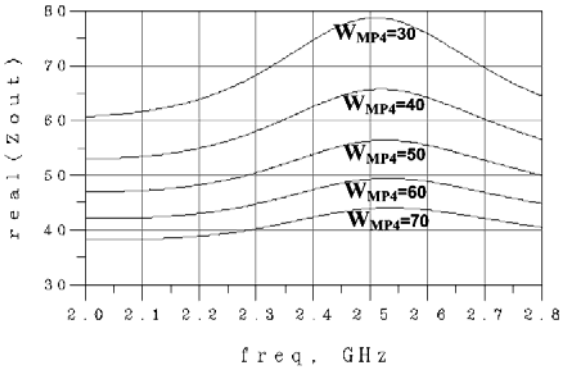

Figure 9. Influence of $W_{MP4}(\mu m)$ on the output impedance.

Equations (6)-(8) indicate that the output impedance depends essentially on g_{mMN2} and R_{MP4}. The variation of these parameters was carried out by the variation of the widths (w) of transistors *MN*2 and *MP*4. Figure 8 and Figure 9 present, respectively, the curves of the output impedance real part versus frequency for different values of W_{MN2} and W_{MP4}.

Figure 8 and Figure 9 indicate that the variation of *gmMN*2 allows a fine adjustment around 50Ω and the variation of *RMP*4 allows a wide adjustment.

2.4. Gain and center frequency

Some other LNA characteristics that are as important as the input and output impedance matching should be studied and analyzed. They are notably the gain and the center frequency of the circuit order necessary to determine the sizing of the LNA.

At the first stage of amplification, the gain of the input matching circuit can be written as follows:

$$G_1 = \frac{pR_{MP2}C_{eq}R_1}{ap^2 + bp + R_B + R_{MP2}}, \tag{9}$$

where a and b are given by (10) and (11), respectively,

$$a = R_1 + R_{MP2} + g_{mMN1}R_1R_{MP2}, \tag{10}$$

$$b = \left((R_1 + R_B + g_{mMN1}R_1R_B)R_{MP2} + R_BR_1\right)C_{eq} + L_B. \tag{11}$$

The gain of the output matching circuit with the second amplification is given by equation (12):

$$G_1 = \frac{pC_{gsMN2}R_2}{1 + pC_{gsMN2}R_2}. \tag{12}$$

The total gain of the circuit is expressed by:

$$G_T = G_2 \times G_1. \tag{13}$$

The expression of the center frequency is obtained from the gain of equation (9) and given by equation (14):

$$f_C = \sqrt{\frac{R_B}{2\Pi R_1\left(\frac{1}{R_B} + \frac{1}{R_{MP2}}\right)C_{eq}L_B\left(\frac{1}{R_1} + \frac{1}{R_{MP2}} + g_{mMN1}\right)}}. \tag{14}$$

Equation (14) shows that the center frequency variation can be achieved when we adjust R_{MP2}, L_B, g_{mMN1}, R_1, C_{eq} and R_B. Compared to the input matching equation (8) in the previous section, we note that we can vary the input impedance by varying R_{MP1} without affecting the center frequency or the gain (equation (13)).

During sizing of the LNA including the input matching circuit, the amplification stage and the output matching circuit are performed as follows:

(i) *MP*2 width is determined by equations (2), (13) and (14) to get the desired bandwidth and we vary *MP*1 width for getting 50Ω at the input.

(ii) *MN*1 width contributes to the bandwidth and the circuit gain but also it has to be small to minimize power consumption and parasitic capacitance.

(iii) According to equations (6) and (7), a better optimization of *MN*2 and *MP*4 widths leads to a good adaptation at the output bearing in mind that *MN*2 has to be small to minimize power consumption and parasitic capacitance.

(iv) The width of the load transistor *MP*3 is determined to obtain a sufficient signal at the output of the first amplifier stage to excite the transistor *MN*2.

(v) Getting a good signal at the output of the LNA is directly dependent on the choice of the *MP*4 width.

(vi) The role of the resistors and capacitors $(R_1, R_2, C_1$ and $C_2)$ is to provide very fine tuning for all LNA features.

3. Simulation Results

The proposed circuit was simulated with 0.18µm standard CMOS process from TSMC. In this part, we validated the proposed techniques and the LNA specifications through simulation. Figure 10 and Figure 11 present, respectively, the simulated voltage gain and the noise figure of the LNA. Simulations show that the LNA has 24.6dB gain at 2.45GHz with 0.98dB

noise figure. Accordingly, the use of transistors instead of resistors reduces the noise. According to Figure 12 and Figure 13, the LNA has a perfect adaptation in the input equal to 50Ω and a better adaptation in the output equal to 49.942Ω at 2.45GHz frequency. At 2.45GHz frequency, Figure 14 and Figure 15 show that the *S*11 parameter is equal to –58.219dB and the *S*22 parameter is equal to –18.294dB. This confirms the good adaptation at the LNA input and output.

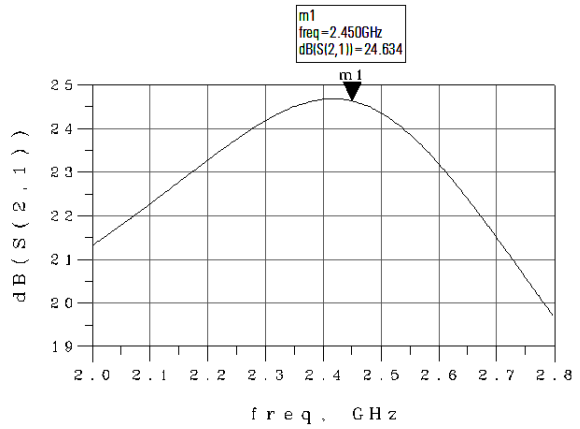

Figure 10. LNA voltage gain.

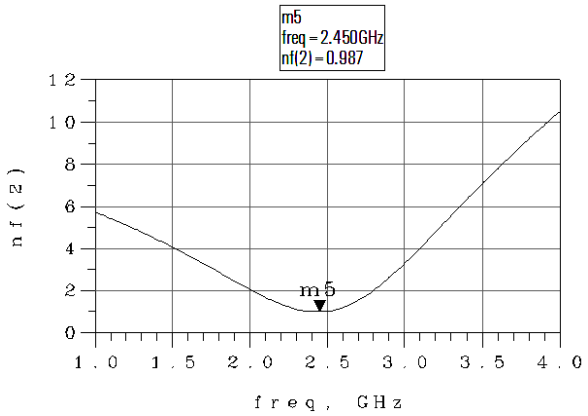

Figure 11. LNA noise figure.

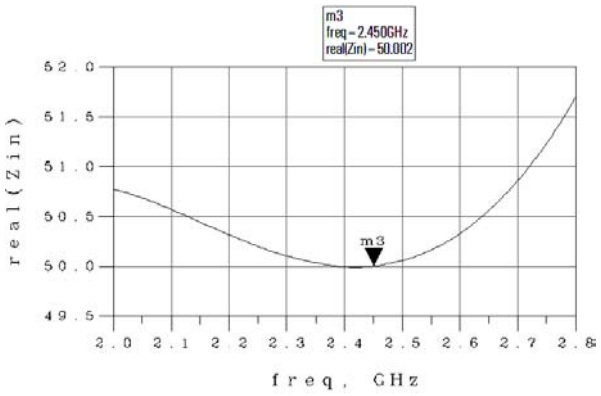

Figure 12. Input impedance real part.

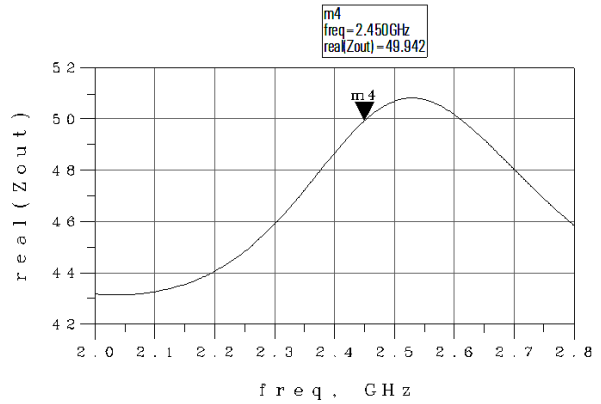

Figure 13. Output impedance real part.

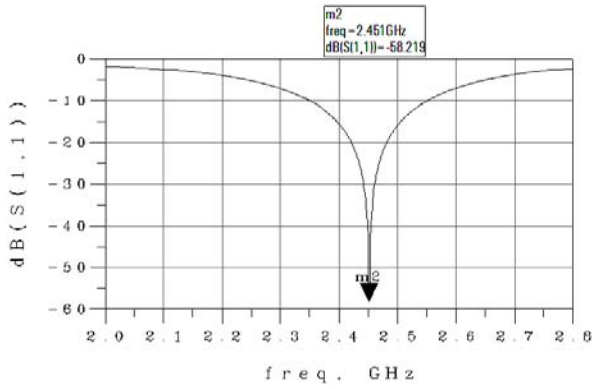

Figure 14. Input reflection coefficient *S*11.

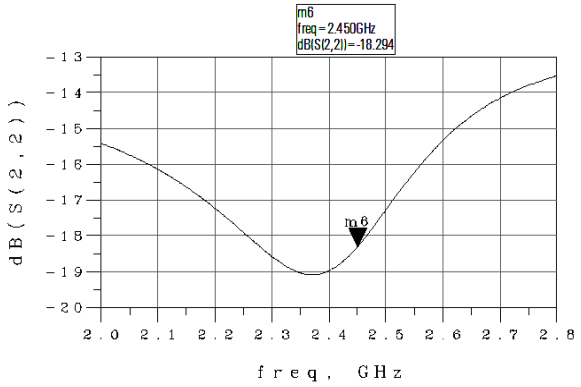

Figure 15. Input reflection coefficient *S*22.

The measurement of the LNA linearity is important because it might be saturated, and this saturation leads to harmonics in the spectrum of the output power. To measure the LNA linearity, we calculated the third intercept point IIP3 presented in Figure 16 and equal to –10dBm, meaning that the designed LNA provides a good linearity.

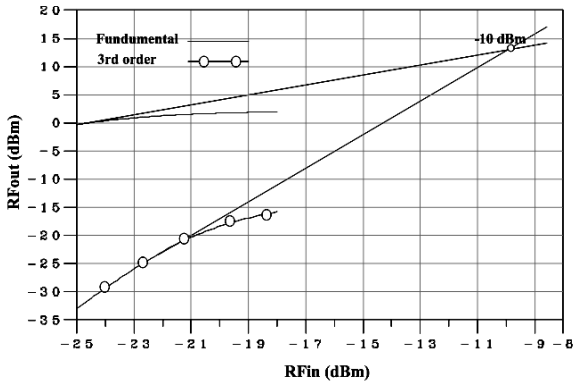

Figure 16. Simulated IIP3 for the proposed LNA.

The system stability was checked by testing whether its factor *K* is greater than 1 [9], and *B* is greater than 0 [3]. The stability coefficients (*K* and *B*) presented in Figure 17 and Figure 18 confirm that *K* is greater than 1 and *B* is greater than 0, so the LNA is perfectly stable.

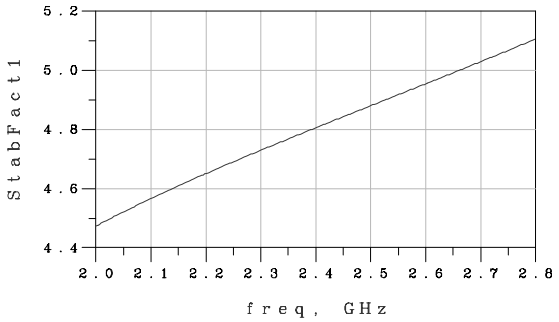

Figure 17. Stability coefficient *K*.

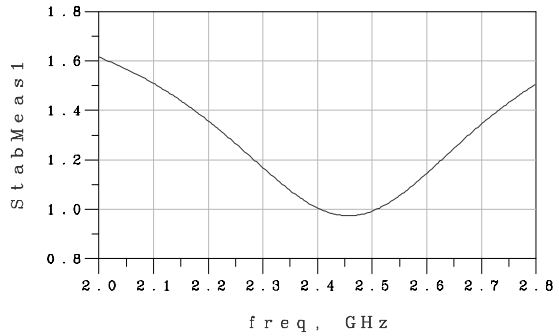

Figure 18. Stability coefficient *B*.

Table 1 lists the performance of the proposed CMOS LNA. And Table 2 gives the characteristics of the proposed LNA compared to the recently published works. This work provides some advantages, such as higher gain, lower noise figure and perfect input and output impedance matching.

Table 1. Summary of LNA's performance

Parameters	Values
*S*21 (dB)	24.634
*S*11 (dB)	–58.22
Real(Zin) (Ω)	50
*S*22 (dB)	–18.294
Real(Zout) (Ω)	49.94
NF (dB)	0.98
IIP3 (dBm)	–10

Table 2. Comparison of the simulated results of the proposed LNA and recently published works

Ref.	[10]	[11]	[12][a]	[13]	This work
Tech (μm)	0.18 CMOS	0.13 CMOS	0.2 CMOS	0.2 CMOS	0.18 CMOS
BW (GHz)	3.1-10.6	3.66	0.9	2.1	2.45
*S*21 (dB)	12.6	14	15.5	16.4	24.6
NF (dB)	3.1-5.7	2	1.65	2.77	0.98
IIP3 (dBm)	–4.2	10.5	22	7.45	–10

[a]Measurement results

4. Conclusion

A new design technique for high gain, low noise and small surface for 2.45GHz low noise amplifier has been developed in 0.18μm CMOS process. This paper presented an effective technique to minimize the noise figure and increase the LNA voltage gain. This technique allows us to use just a single inductor. This, in fact, reduces the size of our circuit. The simulation results show that at 2.45GHz the LNA provides a high voltage gain of about 24.6dB with 0.98dB noise figure and perfect input and output matching impedances, that are equal to 50Ω and 49.94Ω, respectively.

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