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EFFECT OF MOSFET p-n JUNCTION LENGTH ON LEAKAGE CURRENT

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Abstract

For the first time, the effect of every hundredth part of drain (and source) to substrate p-n junction length on OFF and ON current was studied. A numerical relationship between subthreshold leakage current and p-n junction length was proposed. A single NMOS bulk transistor of 20 nm technology generation was simulated by Sentaurus TCAD tool. Simulation result was found in close proximity to the theoretical proposal. Maximum 5613 times reduction in subthreshold leakage current was achieved. A tradeoff between leakage current reduction and ON current loss was also provided as a ready reference for designers to choose among various alternatives for designing low leakage or high speed transistor. As reduction of leakage current was

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done in device level, this methodology can be merged with any circuit level techniques.

1. Introduction

Aggressive demand of smaller size, lower power consumption and better performance in worldwide semiconductor industry is acting as the driving potential for rigorous scaling of CMOS devices for more than 40 years, starting with 10 µm process in 1971 and reaching 22 nm in 2012, conforming Moore's Law [1] and targeting "More-than-Moore" [2]. This results the penalty of terrifying increase of leakage current. The augmentation of leakage current is expected to be 7.5 times for each microprocessor generation [3]. As per the International Technology Roadmap for Semiconductors (ITRS), amount of leakage power is compatible with amount of dynamic power for 65nm node and below [4]. Among the typical six types of leakage components [5], subthreshold leakage current is one of the most significant and governing leakage current [6-10]. Though various researchers are proposing various device level and circuit level solutions for leakage current minimization, but as per the best knowledge of authors, effect of p-n junction length not yet been studied as a tool for leakage minimizing.

In this paper, effect of different p-n junction length is studied. A particular situation is found where ON current loss is less than 10% and OFF current minimization is more than 90% with zero loss in transistor area.

In Section 2 of this paper, numerical relationship between length of p-n junction and subthreshold leakage current is presented. Section 3 describes the methods, Section 4 verifies the relationship by presenting the simulation result of a single N-type MOSFET by Sentaurus TCAD tool. Section 5 concludes the paper.

2. Theoretical Proposal of Numerical Relationship

A. From drain capacitance concept

In short channel MOSFET, not only the gate voltage, but also the drain voltage determines the amount of threshold voltage. The equation of threshold voltage of a short channel MOSFET is given by [11, 12],

$$V_t = V_{t-long} - (V_{ds} + 0.4V) \cdot \frac{C_d}{C_{oxe}}, \quad (1)$$

where V_{t-long} is the threshold voltage for long channel MOSFET, V_{ds} is the applied voltage at drain terminal, C_d is the capacitor between the channel and the drain as shown in Figure 1, and C_{oxe} is the capacitor between the channel and the gate.

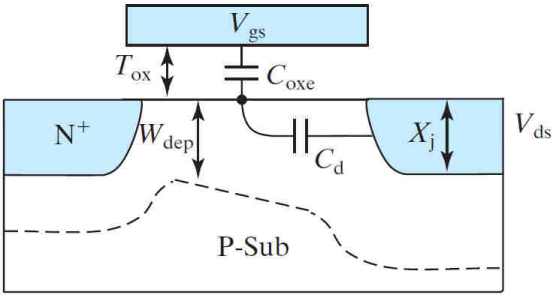

Figure 1. Network of drain and oxide capacitors [11].

From (1), it may be concluded that if C_d is minimized, threshold voltage should increase proportionally if other parameters are kept constant. In [11], it is given that the normal phenomenon of increment of capacitance with decreasing distance of two electrodes is valid for C_d. Similarly it can be said that capacitance would decreases if area of any electrode is minimized.

If an insulator strip is placed just at the drain-substrate p-n junction line, the effective area of drain for C_d is minimized, covering one electrode of the capacitor.

SiO_2 or silicon dioxide is the most common insulating material used in silicon technology. SiO_2 finds its common application as high quality gate oxide and also as electrical insulator in CMOS technology. Silicon dioxide can be formed from silicon very easily and is very much compatible with silicon. It is already in use in silicon CMOS technology. So for the experiment shown in this paper, strip of silicon dioxide is inserted in p-n junction.

Subthreshold current between drain and source is given by [5, 13]:

$$I_{sub} = \mu_0 C_{OX} \frac{W}{L}(m-1)(v_T)^2 \times e^{\frac{V_g - V_{th}}{mv_T}} \times (1 - e^{-\frac{v_{DS}}{v_T}}), \qquad (2)$$

where μ_0 is the mobility at zero bias, C_{OX} is the capacitance of gate oxide, W is the width of channel, L is the length of channel, m is the subthreshold swing coefficient, v_T is thermal voltage, V_g is the applied voltage at gate terminal, V_{th} is the threshold voltage, and V_{DS} is the applied voltage at drain terminal. It is clear from (2) that increase of threshold voltage would exponentially decrease subthreshold leakage current.

So if length of p-n junction is decreased, subthreshold leakage current is expected to decrease exponentially.

B. From depletion capacitance concept

The effect of inserted insulated layer can be understood in another way. As drain region is being insulated, so the effect of drain voltage will be minimized and depletion layer region depth should minimize. Again from the capacitance point of view as depth of depletion layer is distance between two electrodes, decrement of it will increase the value of C_{dep}.

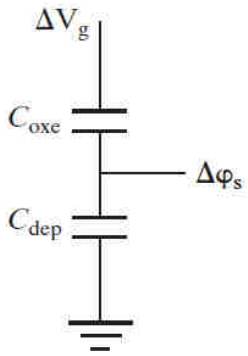

Figure 2. Network of depletion and oxide capacitors [11].

From [11],

$$\frac{d\varphi_s}{dV_{gs}} = \frac{C_{oxe}}{C_{oxe} + C_{dep}} \equiv \frac{1}{\eta}, \tag{3}$$

$$\eta = 1 + \frac{C_{dep}}{C_{oxe}}. \tag{4}$$

Integration of (4) gives

$$\varphi_s = constant + \frac{V_g}{\eta}, \tag{5}$$

$$I_{sub} \propto n_s \propto e^{\frac{q\varphi_s}{kT}} \propto e^{\frac{q\left(constant + \frac{V_g}{\eta}\right)}{kT}} \propto e^{\frac{qV_g}{\eta kT}}. \tag{6}$$

From (4), η increases proportionally with increment of C_{dep}. From (6), as η increases, subthreshold current should decrease exponentially. So, these equations also indicate exponential decrease of leakage current for p-n junction deletion.

C. Disadvantages

If V_t increases, I_{on} is reduced, and delay of gates are increased [11].

$$\tau_d \approx \frac{CV_{dd}}{4}\left(\frac{1}{I_{onN}} + \frac{1}{I_{onP}}\right). \tag{7}$$

3. Methods

As conduction between source and drain is happened in channel area, in this experiment, p-n junction length reduction is done from the other side and is continued up to the gate oxide.

As source and drain terminal are interchangeable in four terminal MOSFET, and the status is determined at the time of operation according to the amount of applied voltage in these terminals, without restricting any normal behavior of transistor and possibility of body biasing engineering, both source and drain p-n junction are insulated symmetrically in this experimental study.

The total length of drain/source-substrate junction line is divided into hundred parts. A strip of SiO_2 was placed in the line having length equal to one hundredth part and width equal to the width of gate oxide. The position of SiO_2 was opposite end of gate oxide. The structure was simulated by Sentaurus TCAD tool and amount of ON and OFF current were noted. Length of the strip was increased by one part and again simulation was conducted. This process was continued until the strip touched gate oxide.

4. Results and Discussions

Figure 3 shows superimpose of conventional and proposed structure. In blue colored substrate region, upper white colored depletion region border belongs to proposed structure and lower one belongs to conventional structure. But in reddish source and drain region, though both borders are situated very closely, upper border belongs to conventional structure and lower one belongs to proposed structure. So in substrate as well as in drain-

source region, proposed structure decreases depletion region area. This is a clear indication of reduction of drain voltage effect.

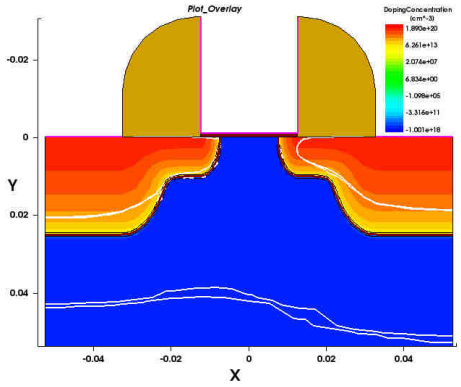

Figure 3. Change in depletion region border and area due to proposed structural change. Applied drain voltage is equal to Vdd and gate voltage is zero.

In Figure 4, orange colored highest electron density region at source and drain is almost same in shape and size with Figure 5. But yellow colored second highest electron density region connects source and drain in Figure 4. In Figure 5, they are not connected by yellow region. This signifies less conduction current in OFF state due to proposed structure.

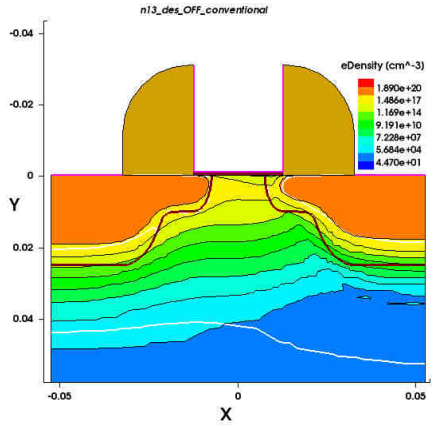

Figure 4. Conventional structure: electron density distribution when gate voltage is zero and drain voltage is equal to Vdd.

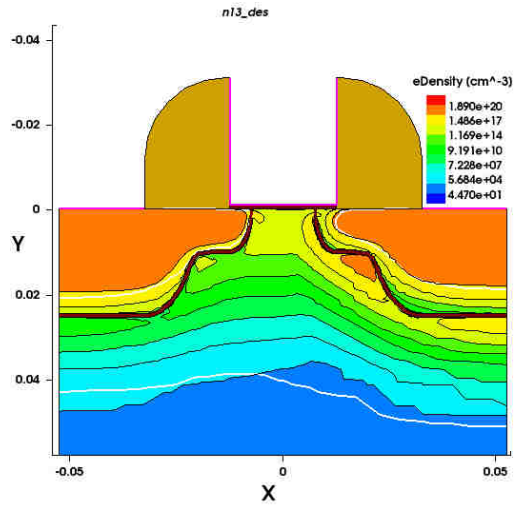

Figure 5. Proposed structure: electron density distribution when gate voltage is zero and drain voltage is equal to Vdd.

In Figure 7, darkest orange segment representing maximum absolute value of total current density is reasonably less compared to conventional structure of Figure 6, when gate voltage of NMOS is zero and transistor is considered as OFF. This confirms less leakage current due to proposed structure.

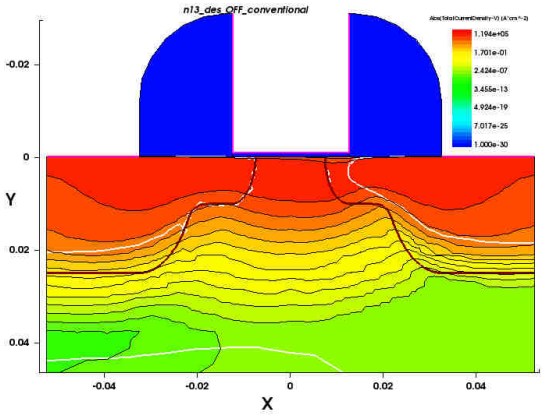

Figure 6. Total current density (absolute value) of conventional structure when drain voltage is equal to Vdd, and gate voltage is equal to zero.

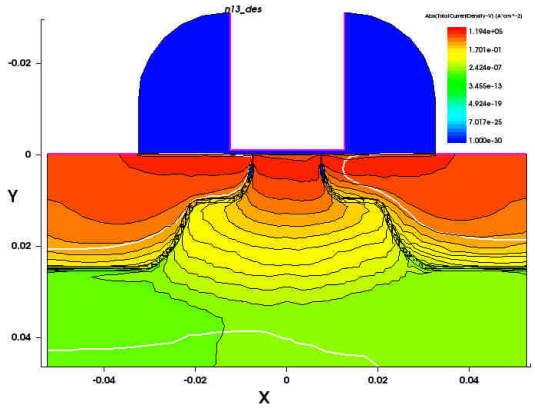

Figure 7. Changed total current density (absolute value) due to proposed structure when drain voltage is equal to Vdd, and gate voltage is equal to zero.

Figure 8 represents the effect of proposed structural change on absolute value of electric field. In drain side red border of conventional structure is visibly more than color band with off-white border belonging to proposed structure. This indicates that electric field strength is weakened due to proposed structure.

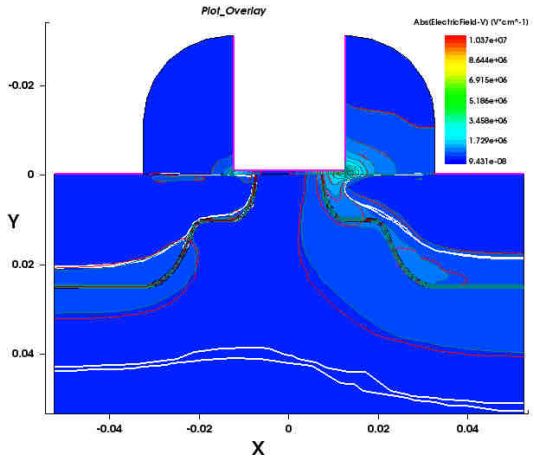

Figure 8. Overlay of conventional and proposed structure for absolute value of electric field. Colored band with off-white border belongs to proposed structure and red border belongs to conventional structure.

Figure 9 shows the simulation result. Continuous line is theoretical calculated value using equation (1) and (2). Amount of leakage current for hundred different length of inserted SiO_2 strip closely follows theoretical line.

Figure 10 shows that ON current is almost independent of p-n junction length reduction except it is very close to gate oxide.

To determine the exact amount of gap required between gate oxide and inserted SiO_2 strip, so that subthreshold leakage current can be reduced sufficiently without harming much ON current, another simulation is done. Taking width of gate oxide as a unit, different gap is produced and simulation is repeated. Table 1 summaries the results.

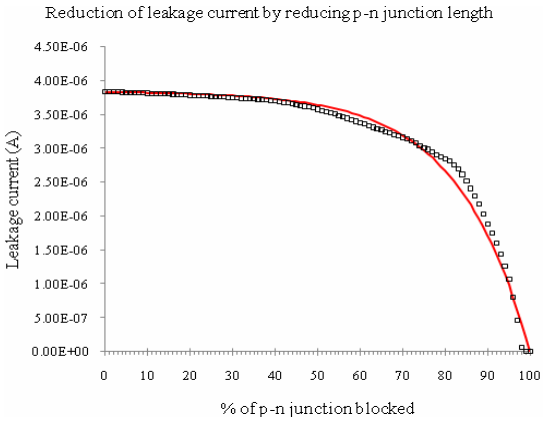

Figure 9. Effect of p-n junction length on leakage current. Black colored boxes represent 100 different simulation results and red colored continuous line represents theoretical expression calculated from equation (1) and (2).

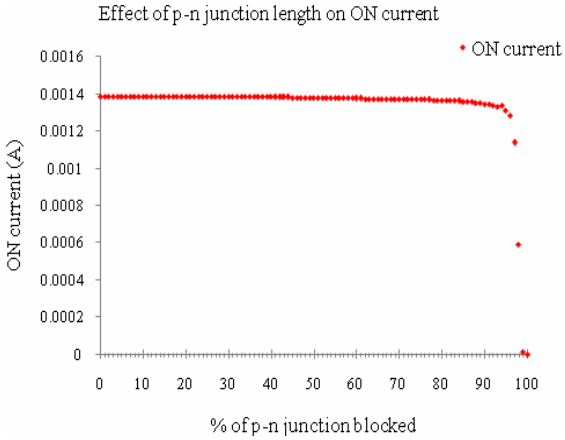

Figure 10. Except channel area, p-n junction length does not effect ON current.

Table 1. Tradeoff between ON and OFF currents

Vertical gap between gate oxide and inserted SiO_2 strip along p-n junction: n times of gate oxide width	% reduction of OFF current	% reduction of ON current
1	99.94%	68.56%
2	96.18%	14.47%
3	**92.17%**	**9.60%**
4	87.47%	7.79%
5	81.52%	6.47%
6	74.64%	5.39%
7	67.55%	4.54%
8	61.24%	3.96%
9	56.39%	3.62%

Table 1 gives a ready reference for designers to choose among high speed (high ON current) or low leakage (low OFF current). As per requirement, any of the configurations can be chosen. Normally a gap three times of the width of gate oxide is recommended. It minimizes leakage current more than 90% and loss of ON current is less than 10%.

5. Conclusion

It may be concluded that subthreshold leakage current becomes very prominent with scaling. If drain (and source) to substrate junction line is reduced by inserting SiO_2 strip there, subthreshold leakage current reduces exponentially. However except channel area, this does not affect the value of ON current. So, calculatedly deletion of p-n junction can minimize sufficient amount of leakage current without losing much ON current.

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